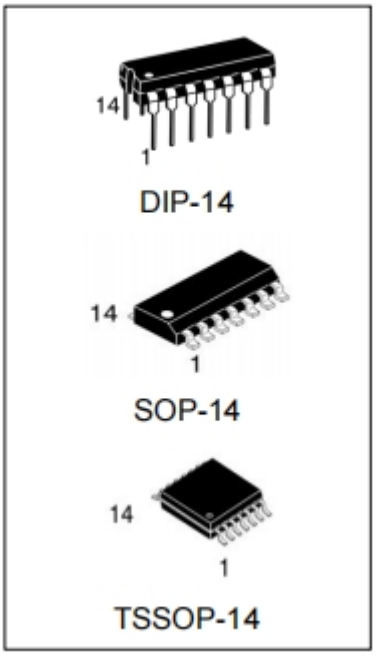
Features

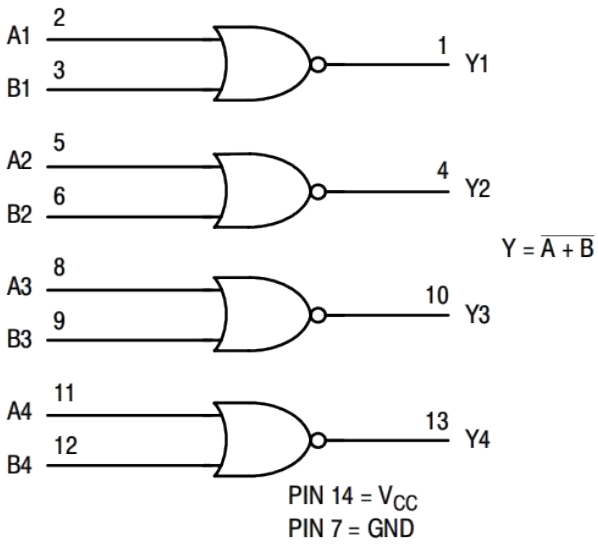
- Output Drive Capability: 10 LSTTLoads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- ESD Performance:
  HBM 2000 V;
  Machine Mode200 V
- Chip Complexity: 40 FETs or 10 Equivalent Gates
- Theseare Pb−Free Devices



Order Information

Product Model	Package Type	Marking	Packing	Packing Qty
74HCO2N	DIP-14	74HC02	TUBE	1000pcs/box
74HC02M/TR	SOP-14	74HC02	REEL	2500pcs/reel
74HCO2MT/TR	TSSOP-14	HC02	REEL	2500pcs/reel

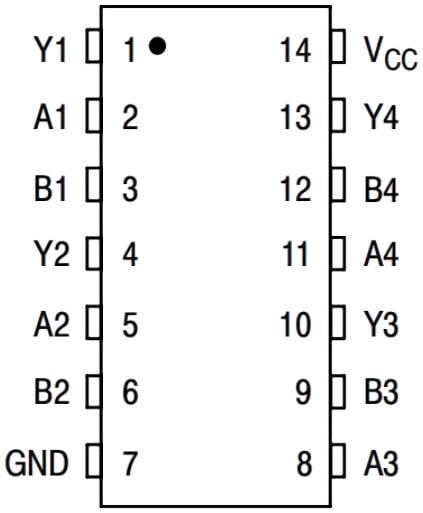
LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

PIN ASSIGNMENT



DIP-14/SOP-14/TSSOP-14

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage(Referenced to GND)	-0.5 to+7.0	V
Vin	DC Input Voltage (Referenced to GND)	-0.5 to VCC+0.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to VCC+0.5	V
Iin	DC Input Current,per Pin	20	mA
Iout	DC Output Current,per Pin	25	mA
IcC	DC Supply Current,VCC and GND Pins	50	mA
PD	Power Dissipation in Still Air,SOP Package TSSOP Package	500 450	mW
Tstg	Storage Temperature	-65 to +150	℃
TL	Lead Temperature,1 mm from Case for 10 Seconds SOP or TSSOP Package	245	℃

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must betaken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance cir-cuit. For proper operation, Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not im-plied. Extended exposure to stresses above the Recommended Operating Conditions may af-fect device reliability.

Derating SOP Package:7 mWfC from 65° to 125° C;TSSOP Package:6.1 mW/C from 65° to 125℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
Vcc	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
Vin,Vout	DC Input Voltage,Output Voltage (Referenced to GND)		0	Vcc	V
TA	Operating Temperature,All Package Types		-40	+85	℃
tr,tf	Input Rise and Fall Time(Figure 1)	VCC=2.0V VCC=4.5V VCC =6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	VCC (V)	Guaranteed Limit			Unit
				-40 to 25℃	≤85℃	≤125℃	
VIH	Minimum High-Level Input Voltage	Vout =0.1 Vor VCC-0.1V |Iout|≤20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
VIL	Maximum Low-Level Input Voltage	Vout =0.1 Vor VCC-0.1V |Iout| ≤20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
VOH	Minimum High-Level OutputVoltage	Vin =VIH or VIL Iout|≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		Vin =VIH or VIL|Iout|≤2.4 mA |Iout|≤4.0 mA Iout|≤5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.7 5.2	
VOL	Maximum Low-Level OutputVoltage	Vin =VIH or VIL |Iout|≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		Vin =VIH or VIL|Iout|≤2.4 mA |Iout|≤4.0 mA Ioutl≤5.2 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
Iin	Maximum Input Leakage Current	Vin =VCC or GND	6.0	0.1	1.0	1.0	μA
Icc	Maximum Quiescent SupplyCurrent (per Package)	Vin =VCC or GND |Ioutl=0μA	6.0	2.0	20	40	μA

AC ELECTRICAL CHARACTERISTICS(CL=50 pF,Inputtr=tf=6.0ns)

Symbol	Parameter	VCC (V)	Guaranteed Limit			Unit
			-40 to 25°C	≤85°C	≤125°C	
tPLH, tPHL	Maximum Propagation Delay,Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
tTLH tTHL	Maximum Output Transition Time,Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
Cin	Maximum Input Capacitance		10	10	10	pF
CPD	Power Dissipation Capacitance (Per Gate)*		Typical @25 C,VCC=5.0 V 22			pF

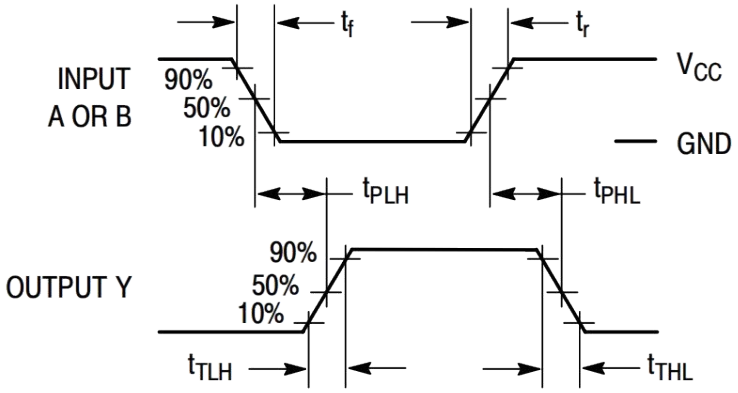
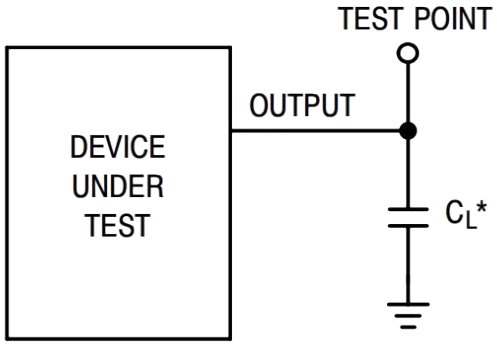


Figure 1.Switching Waveforms



*Includes all probe and jig capacitance

Figure 2.Test Circuit

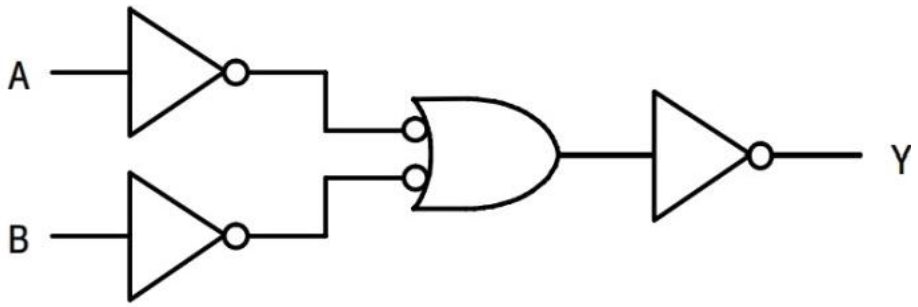
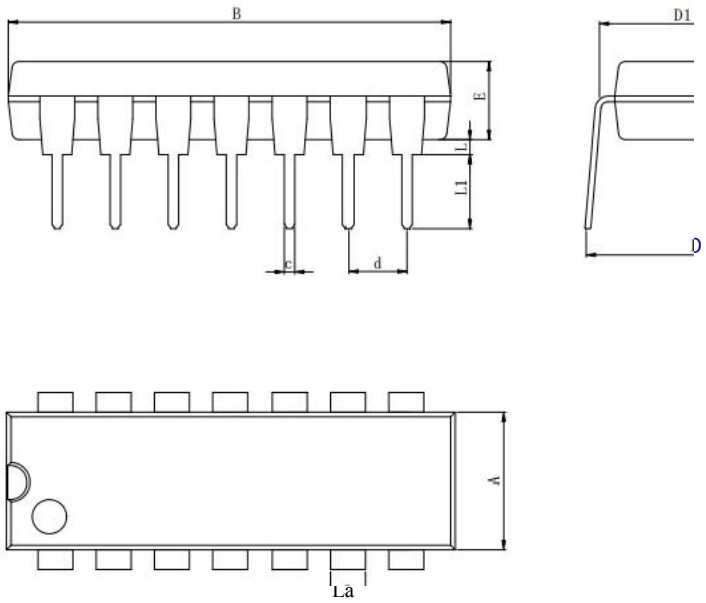


Figure 3. Expanded Logic Diagram
(1/4 of the Device)

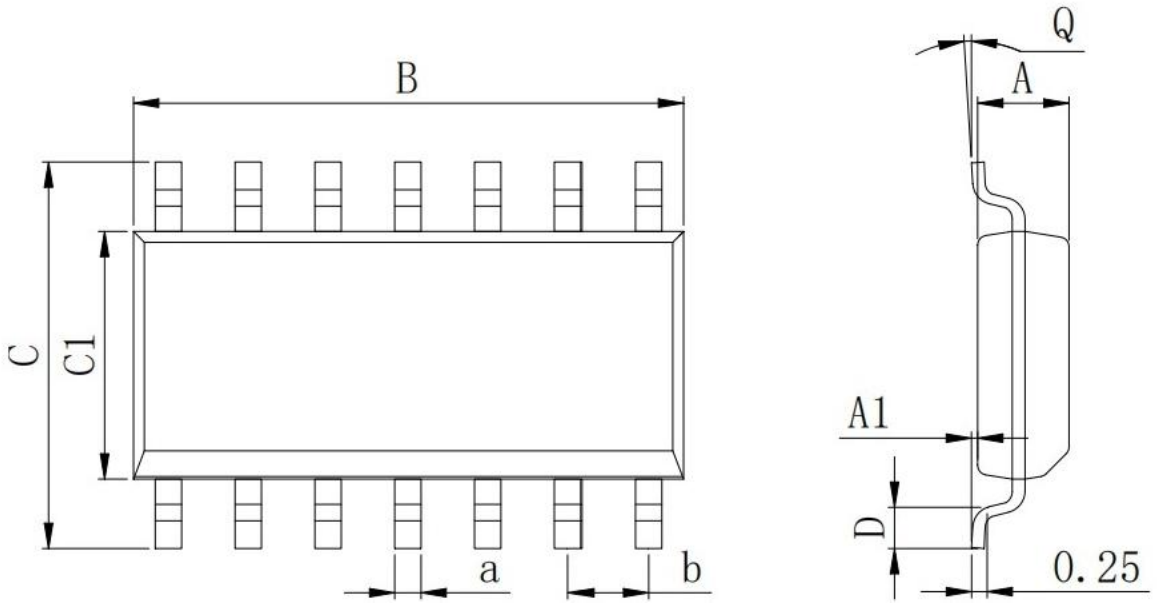
Physical Dimensions

DIP-14



Dimensions In Millimeters(DIP-14)										
Symbol:	**A**	**B**	D	D1	E	L	**L1**	**a**	**C**	**d**
Min:	6.10	**18.94**	8.10	7.42	3.10	**0.50**	**3.00**	**1.50**	**0.40**	**2.54 BSC**
Max:	6.68	**19.56**	10.9	7.82	3.55	**0.70**	**3.60**	**1.55**	**0.50**	

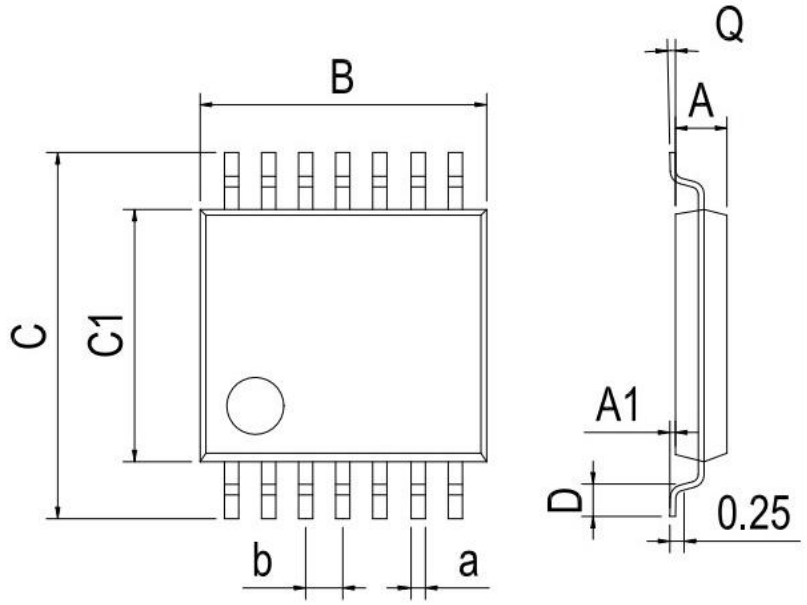
SOP-14



Dimensions In Millimeters(SOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	**0.35**	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	**8°**	**0.45**	

Physical Dimensions

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	**A**	**A1**	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	