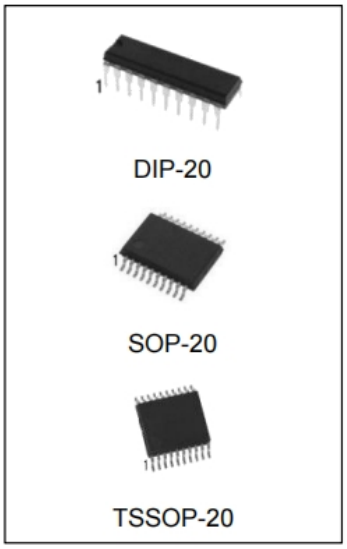
General Description

The 74HC373 is an octal D-type transparent latch with 3-state outputs.The device features latch enable(LE)and output enable($\overline{OE}$)inputs.When LE is HIGH,data at the inputs enter the latches.In this condition the latches are transparent,a latch output will change each time its corresponding D-input changes.When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LoW transition of LE.AHIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.Inputs include clamp diodes.This enables the use of current limiting resistors to interface inputs to voltages in excess of Vcc.

Features

- Input levels:CMOS level
- 3-state non-inverting outputs for bus-oriented applications
- Common 3-state output enable input
- Functionally identical to the 74HC563 and 74HC573
- Specified from -40℃ to +105℃
- Packaging information:DIP-20/SOP-20/TSSOP-20



Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
74HC373N	DIP-20	74HC373	TUBE	720pcs/box
74HC373M/TR	SOP-20	74HC373	REEL	2000pcs/reel
74HC373MT/TR	TSSOP-20	HC373	REEL	2500pcs/reel

Block Diagram

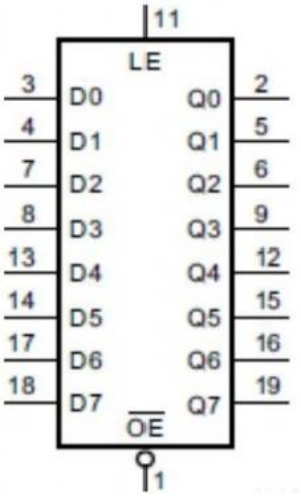


Figure 1.Logic symbol

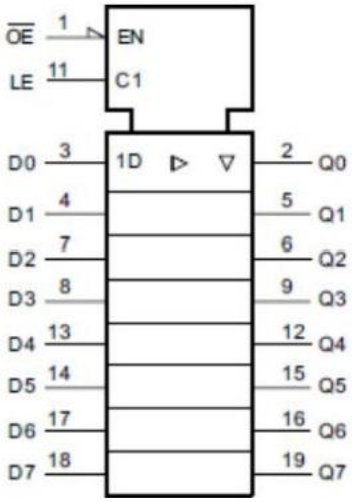


Figure 2.IEC logic symbol

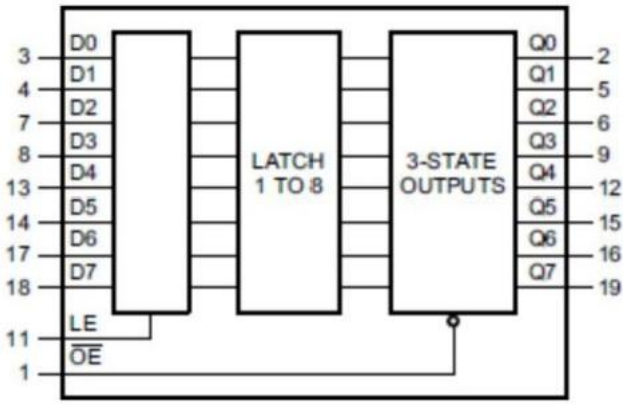


Figure 3.Functional diagram

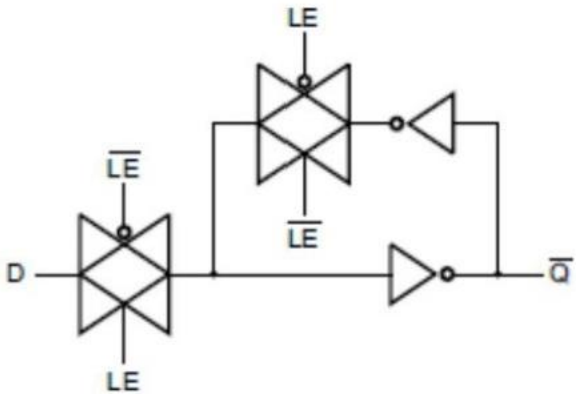


Figure 4.Logic diagram (one latch)

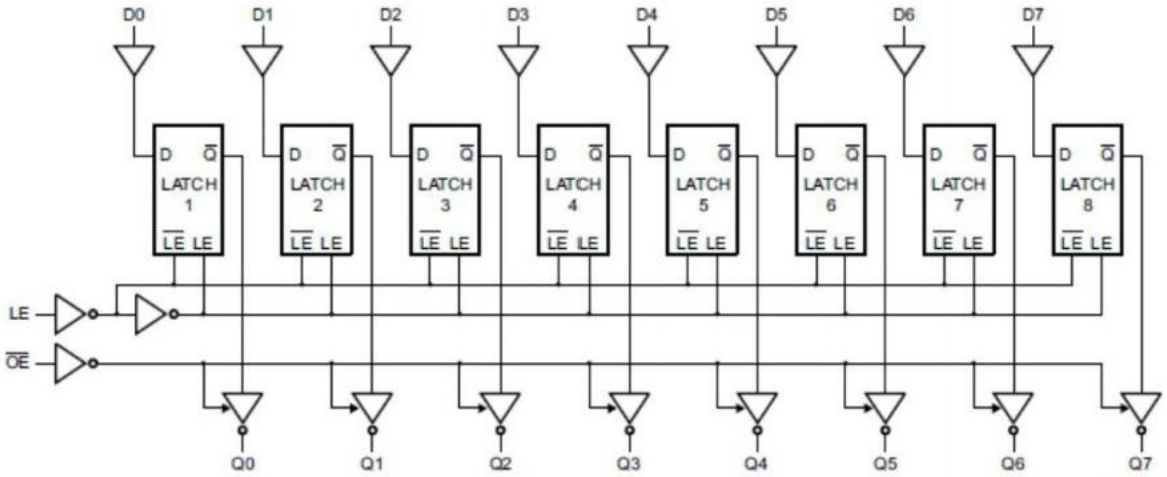
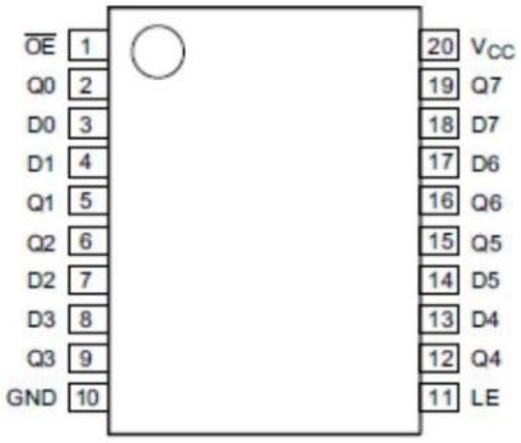


Figure 5.Logic diagram

Pin Configurations



DIP-20/SOP-20/TSSOP-20

Pin Description

Pin No.	Pin Name	Description
1	OE	3-state output enable input (active LOW)
2	Q0	3-state latch output
3	D0	data input
4	D1	data input
5	Q1	3-state latch output
6	Q2	3-state latch output
7	D2	data input
8	D3	data input
9	Q3	3-state latch output
10	GND	ground (0V)
11	LE	latch enable input (active HIGH)
12	Q4	3-state latch output
13	D4	data input
14	D5	data input
15	Q5	3-state latch output
16	Q6	3-state latch output
17	D6	data input
18	D7	data input
19	Q7	3-state latch output
20	Vcc	supply voltage

Function Table

Operating mode	Control		Input	Internal latches	Output
	OE	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	X	X	X	Z

Note: H=HIGH voltage level;L=LOW voltage level;Z=high-impedance OFF-state;X=don't care; h=HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;

l=LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition.

Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V),unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	Vcc			-0.5	+7.0	V
nput clamping current	Ik	VI<-0.5V or V_1>Vcc+0.5V			±20	mA
output clamping current	Iok	Vo<-0.5V or Vo>Vcc+0.5V			±20	mA
output current	Io	Vo=-0.5V to (Vcc+0.5V)			±35	mA
supply current	cc				+70	mA
ground current	IGND			-70		mA
storage temperature	Tstg			-65	+150	℃
total power dissipation	Ptot				500	mW
Soldering temperature	TL	10s	DIP	245		℃
			SOP	245		

Note:1、Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.Operating Ratings indicate conditions for which the device is intended to be functional,but specific performance is not

2、For DIP20 packages:above 70℃ the value of Ptot derates linearly with 12mW/K.

3、For SOP20 packages:above 70℃ the value of Piot derates linearly with 8mW/K.

4、For(T)SSOP20 packages:above 60℃ the value of Piot derates linearly with 5.5mW/K

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	Vcc		2.0	5.0	6.0	V
input voltage	Vi	—	0		Vcc	V
output voltage	Vo		0		Vcc	V
nput transition rise and fall rate	ΔtΔV	Vcc=2.0V			625	nsN
		Vcc=4.5V		1.67	139	nsN
		Vcc=6.0V			83	ns/V
ambient temperature	Tamb		**-40**		+105	℃

Electrical Characteristics

DC Characteristics 1

(Tamb=25℃,voltages are referenced to GND(ground=0V),unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	ViH	Vcc=2.0V		1.5	1.2		V
		Vcc=4.5V		3.15	2.4		V
		Vcc=6.0V		4.2	3.2		V
LOW-level input voltage	VL	Vcc=2.0V			0.8	0.5	V
		Vcc=4.5V			2.1	1.35	V
		Vcc=6.0V			2.8	1.8	V
HIGH-level output voltage	VoH	V_1=Vh or VL	Io=-20uA;Vcc=2.0V	1.9	2.0		V
			Io=-20uA;Vcc=4.5V	4.4	4.5		V
			Io=-20uA;Vcc=6.0V	5.9	6.0		V
			Io=-6.0mA;Vcc=4.5V	3.98	4.32		V
			Io=-7.8mA;Vcc=6.0V	5.48	5.81		V
LOW-level output voltage	Vol	V_1=Vh or VL	Io=20uA;Vcc=2.0V		0	0.1	V
			Io=20uA;Vcc=4.5V		0	0.1	V
			Io=20uA;Vcc=6.0V		0	0.1	V
			Io=6.0mA;Vcc=4.5V		0.15	0.26	V
			Io=7.8mA;Vcc=6.0V		0.16	0.26	V
nput leakage current	h	V=Vcc or GND; Vcc=6.0V				±0.1	uA
OFF-state output current	loz	Vi=Vih or VL;Vcc=6.0V; Vo=Vcc or GND				±0.5	uA
supply current	Icc	V_1=Vcc or GND;Io=0A;Vcc=6.0V				8.0	uA
input **capacitance**	Ci			—	3.5	—	pF

DC Characteristics 2

(Tamb=-40℃ to +85℃,voltages are referenced to GND (ground=0V),unless otherwise specified.)

Parameter	Symbo	Conditions		Min.	Typ	Max	Unit
HIGH-level input voltage	VH	Vcc=2.0V		1.5			V
		Vcc=4.5V		3.15			V
		Vcc=6.0V		4.2			V
LOW-level input voltage	VL	Vcc=2.0V				0.5	V
		Vcc=4.5V				1.35	V
		Vcc=6.0V				1.8	V
HIGH-level output voltage	VoH	Vi=Vih or VL	Io=-20uA;Vcc=2.0V	1.9			V
			Io=-20uA;Vcc=4.5V	4.4			V
			Io=-20uA;Vcc=6.0V	5.9			V
			Io=-6.0mA;Vcc=4.5V	3.84			V
			Io=-7.8mA;Vcc=6.0V	5.34			V
LOW-leve output voltage	Vol	Vi=Vih or VL	Io=20uA;Vcc=2.0V			0.1	V
			Io=20uA;Vcc=4.5V			0.1	V
			Io=20uA;Vcc=6.0V			0.1	V
			Io=6.0mA;Vcc=4.5V			0.33	V
			Io=7.8mA;Vcc=6.0V			0.33	V
input leakage current	I	Vi=Vcc or GND; Vcc=6.0V				±1.0	uA
OFF-state output current	Ioz	Vi=Vih or VL;Vcc=6.0V; Vo=Vcc or GND			-	±5.0	uA
supply current	Icc	V=Vcc or GND;Io=0A;Vcc=6.0V				80	uA

DC Characteristics 3

(Tamb=-40℃ to +105℃,voltages are referenced to GND (ground=0V),unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC373							
HIGH-level input voltage	VH	Vcc=2.0V		1.5			V
		Vcc=4.5V		3.15			V
		Vcc=6.0V		**4.2**			V
LOW-level input voltage	VL	Vcc=2.0V				0.5	V
		Vcc=4.5V				1.35	V
		Vcc=6.0V				1.8	V
HIGH-level output voltage	VoH	V_I=Vih or VL	Io=-20uA;Vcc=2.0V	1.9			V
			Io=-20uA;Vcc=4.5V	4.4			V
			Io=-20uA;Vcc=6.0V	5.9			V
			o=-6.0mA;Vcc=4.5V	3.7			V
			o=-7.8mA;Vcc=6.0V	5.2			V
LOW-level output voltage	VoL	Vi=Vih or VL	Io=20uA;Vcc=2.0V			0.1	V
			Io=20uA;Vcc=4.5V			0.1	V
			Io=20uA;Vcc=6.0V			0.1	V
			Io=6.0mA;Vcc=4.5V			0.4	V
			Io=7.8mA;Vcc=6.0V			0.4	V
input leakage current	I	Vi=Vcc or GND Vcc=6.0V				±1.0	uA
OFF-state output current	loz	Vi=Vih or VL;Vcc=6.0V; Vo=Vcc or GND				±10	uA
supply current	Icc	V=Vcc or GND;Io=0A;Vcc=6.0V				160	uA

AC Characteristics 1

(Tamb=25℃,GND=0V,CL=50pF,unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ	Max.	Unit
propagation delay	tpd	Dn to Qn;see Figure 7	Vcc=2.0V		41	150	NS
			Vcc=4.5V		15	30	NS
			Vcc=5.0V;CL=15pF		12		ns
			Vcc=6.0V		12	26	NS
		LE to Qn;see Figure 8	Vcc=2.0V		50	175	NS
			Vcc=4.5V		18	35	NS
			Vcc=5.0V;Cl=15pF		15		ns
			Vcc=6.0V		14	30	NS
OE to Qn enable time	ten	see Figure 9	Vcc=2.0V		44	150	NS
			Vcc=4.5V		16	30	NS
			Vcc=6.0V		13	26	NS
OE to Qn disable time	tdis	see Figure g	Vcc=2.0V		47	150	NS
			Vcc=4.5V		17	30	NS
			Vcc=6.0V		14	26	NS
transition time	tt	Qn; see Figure 7,8	Vcc=2.0V		14	60	NS
			Vcc=4.5V		5	12	NS
			Vcc=6.0V		4	10	NS
pulse width	tw	LE HIGH; see Figure 8	Vcc=2.0V	80	17		ns
			Vcc=4.5V	16	6		NS
			Vcc=6.0V	14	5		ns
set-up time	tsu	Dn to LE;see Figure 10	Vcc=2.0V	50	14		NS
			Vcc=4.5V	10	5		ns
			Vcc=6.0V	9	4		NS
hold time	th	Dn to LE;see Figure 10	Vcc=2.0V	+5	-8		ns
			Vcc=4.5V	+5	-3		NS
			Vcc=6.0V	+5	-2		ns
power dissipation capacitance	CPD	per latch;VI=GND to Vcc			45		pF

Note:

(1)tpa is the same as tpuhand tpHL.

(2)ten is the same as tpzt and tpzh.

(3)tuis is the same as tpuz and tpHz.

(4)t is the same as trht and tru.

(5)Cpp is used to determine the dynamic power dissipation (PD in uW).

$P_p = C_{PD} \times V_{cc}^2 \times f \times N + \Sigma(C_L \times V_{cc}^2 \times f_o)$ where:

fi=input frequency in MHz; f_o=output frequency in MHz;

C_L=output load capacitance in pF;

Vcc=supply voltage in V;

N=number of inputs switching;

$\Sigma(C_L \times V_{cc}^2 \times f_o)$=sum of outputs.

AC Characteristics 2

(Tamb=-40℃ to+85℃,GND=0V,CL=50pF,unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ	Max	Unit
propagation delay	tpd	Dn to Qn;see Figure 7	Vcc=2.0V			190	NS
			Vcc=4.5V			38	ns
			Vcc=6.0V			33	NS
		LE to Qn;see Figure 8	Vcc=2.0V			220	NS
			Vcc=4.5V			44	NS
			Vcc=6.0V			37	NS
OE to Qn enable time	ten	see Figure 9	Vcc=2.0V			190	ns
			Vcc=4.5V			38	NS
			Vcc=6.0V			33	NS
OE to Qn disable time	tdis	see Figure g	Vcc=2.0V			190	NS
			Vcc=4.5V			38	ns
			Vcc=6.0V			33	ns
transition time	tt	Qn; see Figure 7,8	Vcc=2.0V			75	NS
			Vcc=4.5V			15	NS
			Vcc=6.0V			13	ns
pulse width	tw	LE HIGH; see Figure 8	Vcc=2.0V	100			ns
			Vcc=4.5V	20			NS
			Vcc=6.0V	17			NS
set-up time	tsu	Dn to LE;see Figure 10	Vcc=2.0V	65			NS
			Vcc=4.5V	13			ns
			Vcc=6.0V	11			ns
hold time	th	Dn to LE;see Figure 10	Vcc=2.0V	5			NS
			Vcc=4.5V	5			NS
			Vcc=6.0V	5			ns

Note:
(1)tpa is the same as tph and tpHl.
(2)ten is the same as tpzt and tpzH.
(3)tais is the same as tprz and tp+z.
(4)tt is the same as trhl and trrh

AC Characteristics 3

(Tamb=-40℃ to+105℃, GND=0V, C_1=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC373							
propagation delay	tpd	Dn to Qn;see Figure 7	Vcc=2.0V			225	nS
			Vcc=4.5V			45	ns
			Vcc=6.0V			38	ns
		LE to Qn;see Figure &	Vcc=2.0V			265	NS
			Vcc=4.5V			53	NS
			Vcc=6.0V			45	ns
OE to Qn enable time	ten	see Figure g	Vcc=2.0V			**225**	ns
			Vcc=4.5V			45	NS
			Vcc=6.0V			38	NS
OE to Qn disable time	tdis	see Figure g	Vcc=2.0V			225	NS
			Vcc=4.5V			45	ns
			Vcc=6.0V			38	NS
transition time	tt	Qn; see Figure 7,8	Vcc=2.0V			90	NS
			Vcc=4.5V			18	NS
			Vcc=6.0V			15	ns
pulse width	tw	LE HIGH; see Figure 8	Vcc=2.0V	120			ns
			Vcc=4.5V	24			NS
			Vcc=6.0V	20			NS
set-up time	tsu	Dn to LE;see Figure 10	Vcc=2.0V	75			ns
			Vcc=4.5V	15			ns
			Vcc=6.0V	13			NS
hold time	th	Dn to LE;see Figure 10	Vcc=2.0V	5			NS
			Vcc=4.5V	5			NS
			Vcc=6.0V	5			ns

Note:

(1) tpa is the same as tpuhand tPHL.

(2) ten is the same as tpzr and tPzh.

(3) tais is the same as tpuz and tpHz.

(4) ttis the same as trh and trLh.

Testing Circuit

AC Testing Circuit

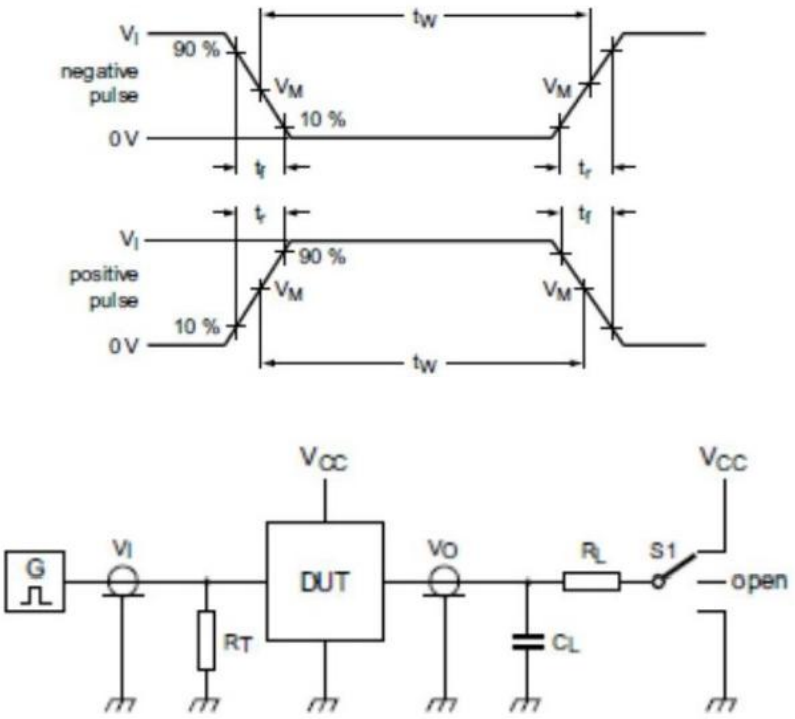


Figure 6. Test circuit for measuring switching times

Definitions for test circuit:

RL=Load resistance.

CL=Load capacitance including jig and probe capacitance.

Rr=Termination resistance should be equal to the output impedance Zo of the pulse generator,

S1=Test selection switch

AC Testing Waveforms

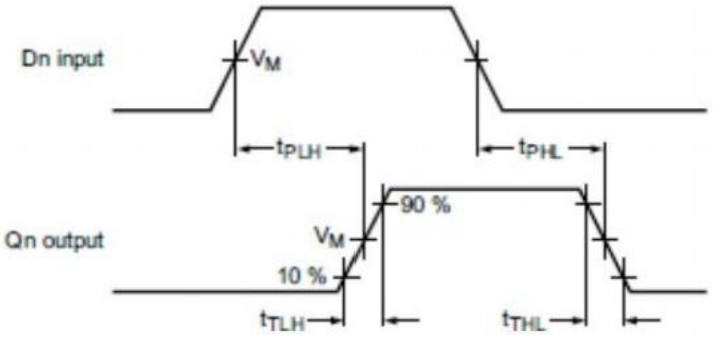


Figure 7. Propagation delay data input (Dn) to output (Qn) and output transition time

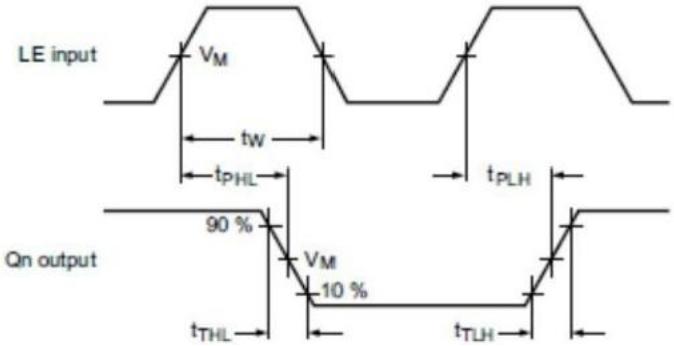


Figure 8. Pulse width latch enable input (LE), propagation delay latch enable input (LE) to output (Qn) and

output transition time

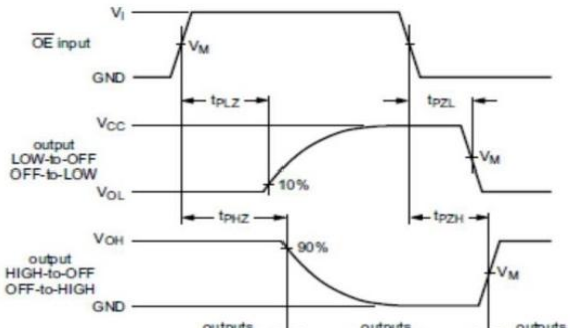


Figure 9. Enable and disable times

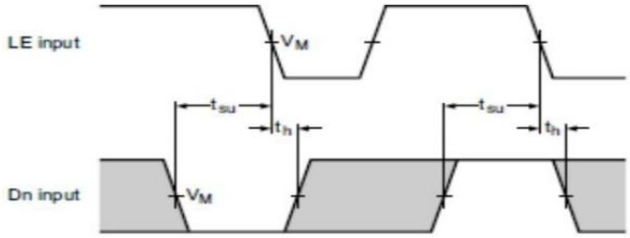


Figure 10. Set-up and hold times for data input (Dn) to latch input (LE)

Measurement Points

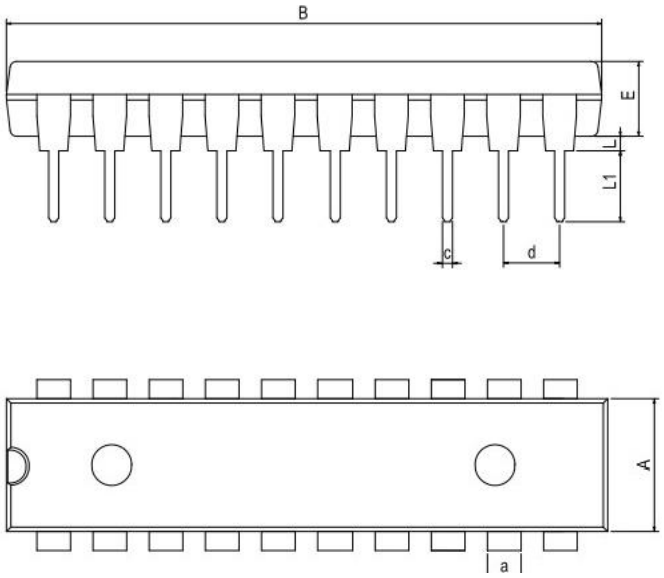
Type	Input	Output
	VM	VM
74HC373	0.5×Vcc	0.5×Vcc

Test Data

Type	Input		Load		S1 position		
	V_I	tr,tr	CL	RL	tpHL, tpLH	tpzH, tpHz	tpuz
74HC373	Vcc	6ns	15pF,50pF	1kΩ	open	GND	Vcc

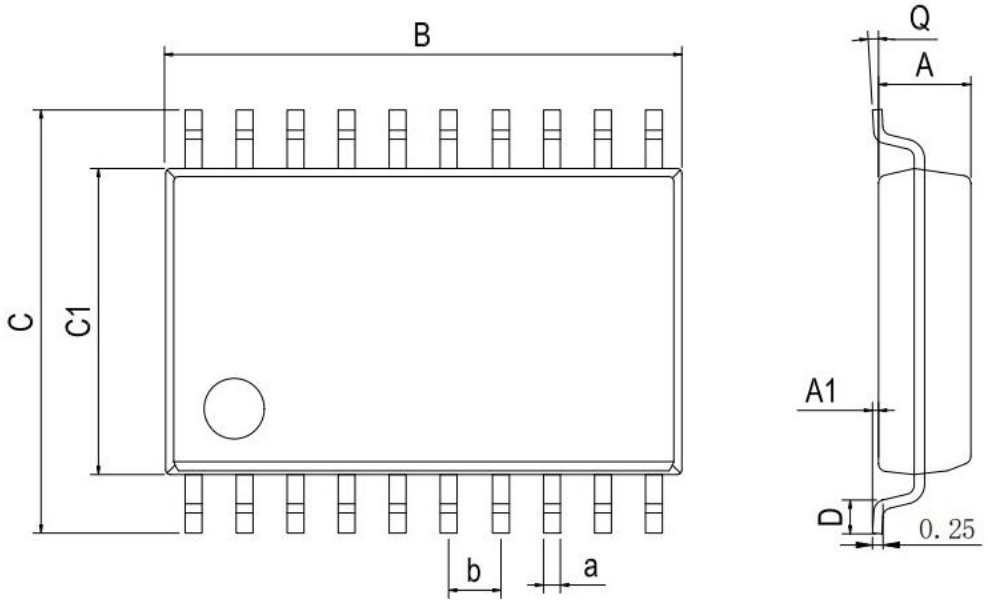
Physical Dimensions

DIP-20



Dimensions In Millimeters(DIP-20)										
Symbol:	A	B	D	D1	E	L	**L1**	**a**	**C**	**d**
Min:	6.10	24.95	8.10	7.42	3.10	0.50	**3.00**	**1.50**	**0.40**	**2.54 BSC**
Max:	6.68	26.55	10.9	7.82	3.55	0.70	**3.60**	**1.55**	**0.50**	

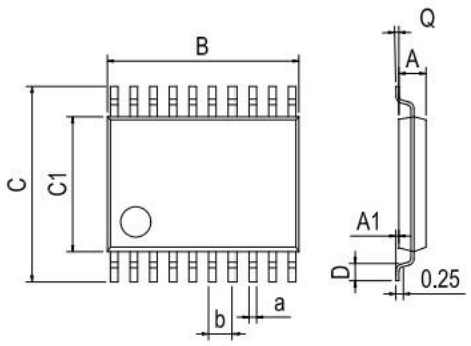
SOP-20



Dimensions In Millimeters(SOP-20)									
Symbol:	**A**	**A1**	B	C	**C1**	**D**	**Q**	**a**	**b**
Min:	2.10	0.05	12.50	10.21	**7.40**	**0.45**	**0°**	**0.35**	**1.27 BSC**
Max:	2.50	0.25	13.00	10.61	**7.60**	**1.25**	**8°**	**0.45**	

Physical Dimensions

TSSOP-20



Dimensions In Millimeters(TSSOP-20)									
Symbol:	**A**	**A1**	**B**	C	C1	**D**	**Q**	**a**	**b**
Min:	0.85	0.05	6.40	6.20	4.30	**0.40**	**0°**	**0.20**	**0.65 BSC**
Max:	1.05	0.20	6.60	6.60	**4.50**	**0.80**	**8°**	**0.25**	