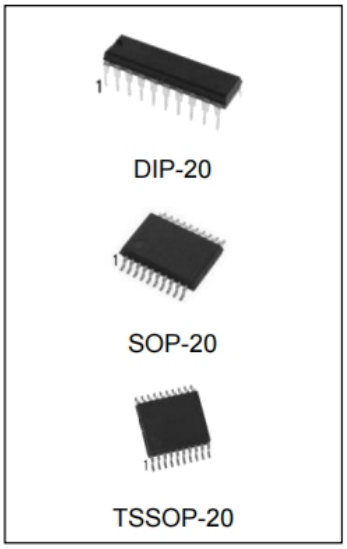
General Description

The 74HC/HCT374 is an octal positive-edge triggered D-type flip-flop with 3-state outputs. Thedevice features a clock (CP) and output enable (OE) inputs. The flip-flops will store the state of theirindividual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP)transition. A HIGH on OE causes the outputs to assume a high-impedance OFF-state. Operation of the OE input does not affect the state of the flip-flops. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of VCC. The 74HCT374 features reduced input threshold levels to allow interfacing to TTL logic levels.

Features

- Input levels:
  For 74HC374:CMOS level
  For 74HCT374:TTL level
- Octal bus interface
- Non-inverting 3-state outputs
- 8-bit positive,edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Specified from-40℃ to +85℃
- Packaging information:DIP-20/SOP-20/TSSOP-20



Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
74HC374N	DIP-20	74HC374	TUBE	720pcs/box
74HCT374N	DIP-20	74HCT374	TUBE	720pcs/box
74HC374M/TR	SOP-20	74HC374	REEL	2000pcs/reel
74HCT374M/TR	SOP-20	74HCT374	REEL	2000pcs/reel
74HC374MT/TR	TSSOP-20	HC374	REEL	2500pcs/reel
74HCT374MT/TR	TSSOP-20	HCT374	REEL	2500pcs/reel

Block Diagram

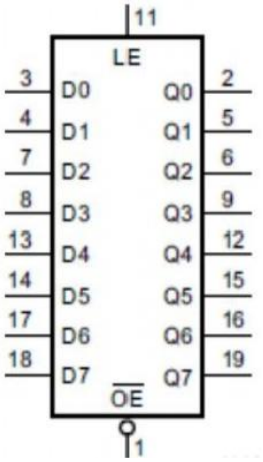


Figure 1.Logic symbol

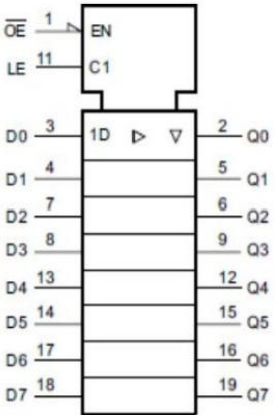


Figure 2.IEC logic symbol

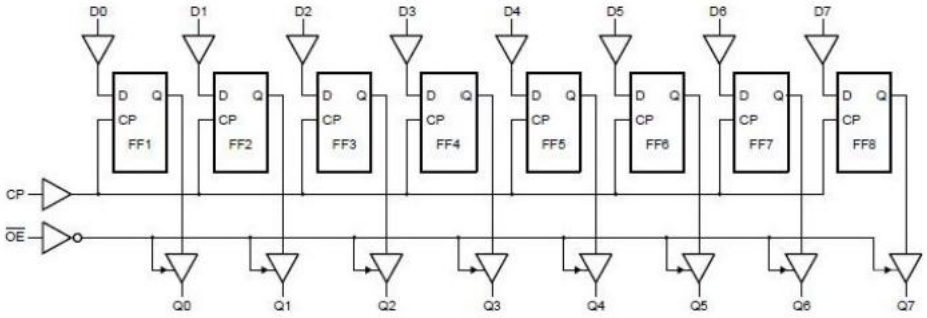


Figure 3.Logic diagram

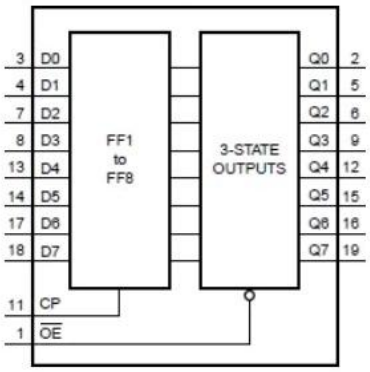
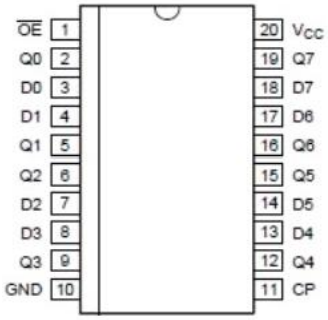


Figure 4.Functional diagram

Pin Configurations



Pin Description

Pin No	Pin Name	Description	Pin No.	Pin Name	Description
1	OE	output enable input (active LOW)	11	CP	clock input (LOW-to-HIGH edge-triggered)
2	Q0	data output	12	Q4	data output
3	DO	data input	13	D4	data input
4	D1	data input	14	D5	data input
5	Q1	data output	15	Q5	data output
6	Q2	data outpu	16	Q6	data outpu
7	D2	data input	17	D6	data input
8	D3	data input	18	D7	data inpu
9	Q3	data output	19	Q7	data output
10	GND	ground (0V)	20	Vcc	supply voltage

Function Table

Operating modes	Input			Internal flip-flops	Output
	OE	CP	Dn		Qn
Load and read register	L	↑		L	L
	L	↑	h	H	H
Load register and disable outputs	H			L	Z
	H	↑	h	H	Z

Note:H=HIGH voltage level;L=LOW voltage level;X=don't care;Z=high-impedance OFF-state;
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
↑=LOW-to-HIGH clock transition.

Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V),unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Max	Unit
supply voltage	VCC			-0.5	+7.0	V
input clampingcurrent	IIK	Vi<-0.5V or V_1>Vcc+0.5V			±20	mA
output clampingcurrent	IOK	Vo<-0.5V or Vo>Vcc+0.5V			±20	mA
output current	Io	-0.5V<Vo<Vcc+0.5V			±35	mA
supply current	Icc				70	mA
ground cumen	IGND			-70		mA
storage temperature	Tstg			-65	+150	℃
total powerdissipation	Ptot				500	mW
Soldering temperature	TL	10s	DIP	245		℃
			SOP	245		

Note:1、Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.Operating Ratings indicate conditions for which the device is intended to be functional,but specific performance is not ensured.

2、For DIP20 packages:above 70℃ the value of Pot derates linearly with 12mW/K.

3、For SOP20 packages:above 70℃ the value of Put derates linearly with 8mWIK.

4、ForTSSOP20 packages:above 60℃ the value of Put derates linearly with 5.5mW/K.

Recommended Operationg Conditions

74HC374

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
supply voltage	VCC		2.0	5.0	6.0	V
input voltage	Vi		0		VCC	V
output voltage	Vo		0		Vcc	V
Input transitionrise and fall rate	ΔtΔV	Vcc=2.0V			625	ns/V
		Vcc=4.5V		1.67	139	nsV
		Vcc=6.0V			83	nsV
ambient emperature	Tamb		-40		+85	℃
supply voltage	VCC		**4.5**	5.0	5.5	V
input voltage	V_1		0		VcC	V
output voltage	Vo		0		VCC	V
input transitionrise and fall rate	ΔtΔV	Vcc=2.0V				ns/V
		Vcc=4.5V		1.67	139	ns/V
		Vcc=6.0V				nsV
ambient temperature	Tamb		-40		+85	℃

Electrical Characteristics

DC Characteristics 1

(Tamb=25℃, voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC374							
HIGH-level input voltage	VIH	Vcc=2.0V		1.5	1.2		V
		Vcc=4.5V		3.15	2.4		V
		Vcc=6.0V		4.2	3.2		V
LOW-leve input voltage	VL	Vcc=2.0V			0.8	0.5	V
		Vcc=4.5V			2.1	1.35	V
		Vcc=6.0V			2.8	1.8	V
HIGH-level output voltage	VoH	V=Vih or VL	Io=-20uA;Vcc=2.0V	1.9	2.0		V
			Io=-20uA;Vcc=4.5V	4.4	4.5		V
			Io=-20uA;Vcc=6.0V	5.9	6.0		V
			Io=-6.0mA;Vcc=4.5V	3.98	4.32		V
			Io=-7.8mA;Vcc=6.0V	5.48	5.81		V
LOW-level output voltage	VOL	V=Vih or VL	Io=20uA;Vcc=2.0V		0	0.1	V
			Io=20uA;Vcc=4.5V		0	0.1	V
			Io=20uA;Vcc=6.0V		0	0.1	V
			Io=6.0mA;Vcc=4.5V		0.15	0.26	V
			Io=7.8mA;Vcc=6.0V		0.16	0.26	V
input leakage current	I	V=Vcc or GND;Vcc=6.0V				±0.1	uA
OFF-state output current	Ioz	V=Vih or VL;Vcc=6.0V; Vo=Vcc or GND				±0.5	uA
supply curren	ICC	V=Vcc or GND;Io=0A;Vcc=6.0V				8.0	uA
input capacitance	C				3.5		pF
74HCT374							
HIGH-level input voltage	VIH	Vcc=4.5V to 5.5V		2.0	1.6		V
LOW-level input voltage	VIL	Vcc=4.5V to 5.5V			1.2	0.8	V
HIGH-level output voltage	VOH	V=Vih or VL; Vcc=4.5V	o=-20uA	4.4	4.5		V
			Io=-6.0mA	3.98	4.32		V
LOW-level	VOL	V_I=VH or VL;	o=20uA		0	0.1	V
output voltage		Vcc=4.5V	Io=6.0mA		0.16	0.26	V
input leakage current	I	Vi=Vcc or GND;Vcc=5.5V				±0.1	uA
OFF-state output current	Ioz	Vi=Vih or VL;Vcc=5.5V;Vo=Vcc or GND				±0.5	uA
supply current	IcC	V=Vcc or GND;Io=0A;Vcc=5.5V				8.0	uA
additional supply current	ΔIcc	per input pin; Vi=Vcc-2.1V other inputs at Vccor GND;Io=0A; Vcc=4.5V to 5.5V	OE input		125	450	uA
			CP input		90	324	uA
			Dn input		35	126	uA
nput capacitance	Ci				3.5		pF

DC Characteristics 2

(Tamb=-40℃ to +85℃,voltages are referenced to GND (ground=0V),unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
74HC374							
HIGH-level input voltage	VIH	Vcc=2.0V		1.5			V
		Vcc=4.5V		3.15			V
		Vcc=6.0V		4.2			V
LOW-level nput voltage	VIL	Vcc=2.0V				0.5	V
		Vcc=4.5V				1.35	V
		Vcc=6.0V				1.8	V
HIGH-level output voltage	VOH	V_1=Vih or VL	Io=-20uA;Vcc=2.0V	1.9			V
			Io=-20uA;Vcc=4.5V	4.4			V
			Io=-20uA;Vcc=6.0V	5.9			V
			Io=-6.0mA;Vcc=4.5V	3.84			V
			Io=-7.8mA;Vcc=6.0V	5.34			V
LOW-level output voltage	VOL	V_1=ViH or VL	Io=20uA;Vcc=2.0V			0.1	V
			Io=20uA;Vcc=4.5V			0.1	V
			Io=20uA;Vcc=6.0V			0.1	V
			Io=6.0mA;Vcc=4.5V			0.33	V
			Io=7.8mA;Vcc=6.0V			0.33	V
input leakage current	I	V=Vcc or GND;Vcc=6.0V				±1.0	uA
OFF-state output current	IOZ	V_1=ViH or VL;Vcc=6.0V;Vo=Vcc or GND				±5.0	uA
supply current	Icc	Vi=Vcc or GND;Io=0A;Vcc=6.0V				80	uA
input capacitance	Ci						pF
74HCT374							
HIGH-level input voltage	VIH	Vcc=4.5V to 5.5V		2.0			V
LOW-level	VIL	Vcc=4.5V to 5.5V				0.8	V
input voltage							
HIGH-leve output voltage	VOH	V_1=Vih or VL; Vcc=4.5V	Io=-20uA	4.4			V
			Io=-6.0mA	3.84			V
LOW-level output voltage	VOL	V_1=Vih or Vμ; Vcc=4.5V	Io=20uA			0.1	V
			o=6.0mA			0.33	V
input leakage current		Vi=Vcc or GND;Vcc=5.5V				±1.0	uA
OFF-state output current	Ioz	V=Vih or VL;Vcc=5.5V;Vo=Vcc or GND				±5.0	uA
supply current	Icc	V=Vcc or GND;Io=0A;Vcc=5.5V				80	uA
additional supply current	ΔIcc	per input pin; V_1=Vcc-2.1V; other inputs at Vccor GND;Io=0A;Vcc=4.5V to 5.5V	OE input			563	uA
			CP input			405	uA
			Dn input			158	uA
input capacitance	C_1						pF

AC Characteristics 1

(Tamb=25℃,voltages are referenced to GND (ground=0V),unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
74HC374							
CP to Qn propagationdelay	tpd	see Figure 6	Vcc=2.0V		50	165	ns
			Vcc=4.5V		18	33	ns
			Vcc=5.0V;CL=15pF		15		ns
			Vcc=6.0V		14	18	ns
OE to Qn enable time	ten	see Figure 7	Vcc=2.0V		41	150	ns
			Vcc=4.5V		15	30	NS
			Vcc=6.0V		12	26	ns
OE to Qn disable time	tdis	see Figure 7	Vcc=2.0V		50	150	ns
			Vcc=4.5V		18	30	ns
			Vcc=6.0V		14	26	ns
transition time	t	Qn output; see Figure 6	Vcc=2.0V		14	60	ns
			Vcc=4.5V		5	12	ns
			Vcc=6.0V		4	10	ns
pulse width	tw	CP;HIGH orLOW; see Figure 6	Vcc=2.0V	80	19		NS
			Vcc=4.5V	16			ns
			Vcc=6.0V	14	6		ns
Dn to CP set-up time	tsu	see Figure 6	Vcc=2.0V	60	14		ns
			Vcc=4.5V	12	5		ns
			Vcc=6.0V	10	4		ns
Dn to CPhold time	th	see Figure 6	Vcc=2.0V	5	-6		ns
			Vcc=4.5V	5	-2		ns
			Vcc=6.0V	5	-2		ns
maximum frequency	fmax	CP input;see Figure 6	Vcc=2.0V	6.0	23		MHz
			Vcc=4.5V	30	70		MHz
			Vcc=5.0V;C_1=15pF		77		MHz
			Vcc=6.0V	35	83		MHz
power dissipation capacitance	CPD	per flip-flop;V=GND to Vcc			17		pF
CP to Qn propagationdelay	tpd	see Figure 6	Vcc=4.5V		16	32	ns
			Vcc=5.0V;C_1=15pF		13		ns
OE to Qn enable time	ten	Vcc=4.5V;see Figure 7			16	30	ns
OE to Qn disable time	tdis	Vcc=4.5V;see Figure 7			18	28	ns
transition time	t	Qn;Vcc=4.5V;see Figure 6			5	12	**ns**
pulse width	tw	CP;HIGH orLOW; Vcc=4.5V;see Figure 6		19	11		ns
Dn to CP set-up time	tsu	Vcc=4.5V;see Figure 6		12	7		ns
Dn to CPholo time	tn	Vcc=4.5V;see Figure 6		5	-3		ns
maximum frequency	fmax	CP input; see Figure 6	Vcc=4.5V	26	44		MHz
			Vcc=5.0V;Ci=15pF		48		MHz
power dissipation capacitance	CPD	per flip-flop;V=GND to Vcc-1.5V			17		pF

Note:

1.tpa is the same as tpurandtpHl.

2.ten is the same as tpzrand tpzh.

3.tis is the same as tpuzandtpHz.

4.t is the same as tru and trun.

5.Cpo is used to determine the dynamic power dissipation (Po in uW).

Po=Cpp×V 2×fi×N+Z(CL×Vcc²×fo)where: fi=input frequency in MHz;

fo=output frequency in MHz;

C_1=output load capacitance in pF;

Vcc=supply voltage in V;

N=number of inputs switching;

Z(C_1×Vcc²×fo)=sum of outputs.

AC Characteristics 2

(Tamb=-40℃ to +85℃,voltages are referenced to GND (ground=0V),unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ	Max.	Unit
74HC374							
CP to Qn propagation delay	tpd	see Figure 6	Vcc=2.0V		_	205	ns
			Vcc=4.5V			41	ns
			Vcc=5.0V;C_1=15pF				ns
			Vcc=6.0V			35	ns
0F to Qn enable time	ten	see Figure 7	Vcc=2.0V			190	ns
			Vcc=4.5V			38	NS
			Vcc=6.0V			33	ns
OF to Qn disable time	tdis	see Figure 7	Vcc=2.0V			190	ns
			Vcc=4.5V			38	NS
			Vcc=6.0V			33	ns
transition time	t	Qn output; see Figure 6	Vcc=2.0V			75	ns
			Vcc=4.5V			15	NS
			Vcc=6.0V			13	1S
pulse width	tw	CP;HIGH orLOW; see Figure 6	Vcc=2.0V	100			ns
			Vcc=4.5V	20			ns
			Vcc=6.0V	17			ns
Dn to CP set-up time	tsu	see Figure 6	Vcc=2.0V	75			ns
			Vcc=4.5V	15			ns
			Vcc=6.0V	13			ns
Dn to CPhold time	tn	see Figure 6	Vcc=2.0V	5			ns
			Vcc=4.5V	5			ns
			Vcc=6.0V	5			ns
maximumfrequency	fmax	CP input; see Figure 6	Vcc=2.0V	4.8			MHz
			Vcc=4.5V	24			MHz
			Vcc=5.0V;C_1=15pF				MHz
			Vcc=6.0V	28			MHz
power dissipation capacitance	CPD	per flip-flop;V_1=GND to Vcc					pF

74HCT374

CP to Qn propagation delay	tpd	see Figure 6	Vcc=4.5V			40	ns
			Vcc=5.0V;C_1=15pF				NS
OE to Qn enable time	ten	Vcc=4.5V;see Figure 7				38	NS
OE to Qn disable time	tdis	Vcc=4.5V;see Figure 7				35	NS
transition time	t	Qn;Vcc=4.5V;see Figure 6				15	ns
pulse width	tw	CP;HIGH or LOW Vcc=4.5V;see Figure 6		24			ns
Dn to CP set-up time	tsu	Vcc=4.5V;see Figure 6		15			ns
Dn to CP hold time	tn	Vcc=4.5V;see Figure 6		5		—	ns
maximumfrequency	fmax	CP input;see Figure 6	Vcc=4.5V	21			MHz
			Vcc=5.0V;CL=15pF				MHz
power dissipationcapacitance	CPD	per flip-flop;V=GND to Vcc-1.5V					pF

Note:

6.tpd is the same as tpuhand tpHl.

7.ten is the same as tpzt and tpzH.

8.tis is the same as tprzandtpHz.

9.t is the same as trhland trLh.

10.Cpo is used to determine the dynamic power dissipation (Po in uW).

Po=Cpp×V 2×fi×N+Z(CL×Vcc²×fo)where:

fi=input frequency in MHz;

fo=output frequency in MHz;

CL=output load capacitance in pF;

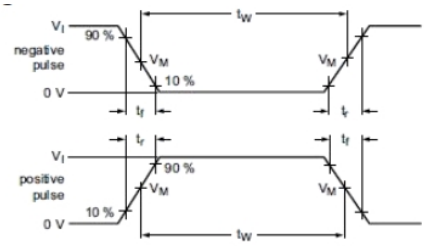
Vcc=supply voltage in V;

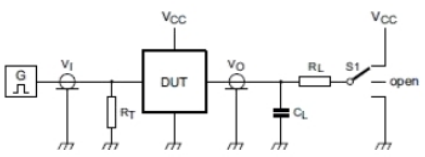
N=number of inputs switching;

Z(CL×Vcc²×fo)=sum of outputs.

Testing Circuit

AC Testing Circuit





Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.S1=Test selection switch.

Figure 5. Test circuit for measuring switching times

AC Testing Waveforms

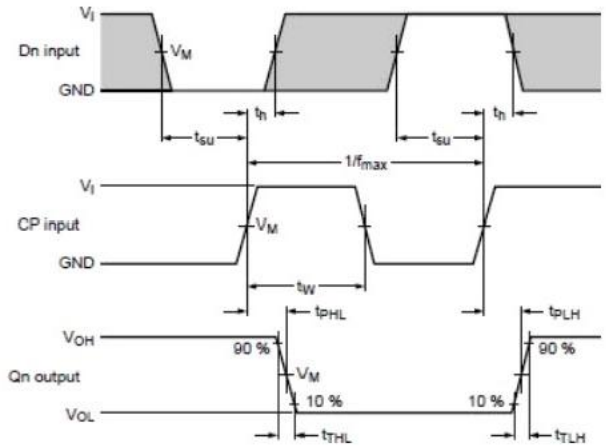


Figure 6. Clock input (CP) to output (Qn) propagation delay, clock pulse width, data (Dn) to clock (CP) set-up and hold times, output transition times (Qn) and maximum clock frequency

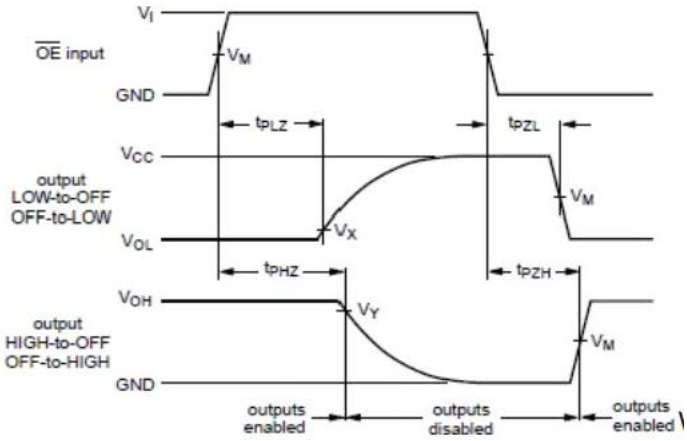


Figure 7. 3-state enable and disable times

Measurement Points

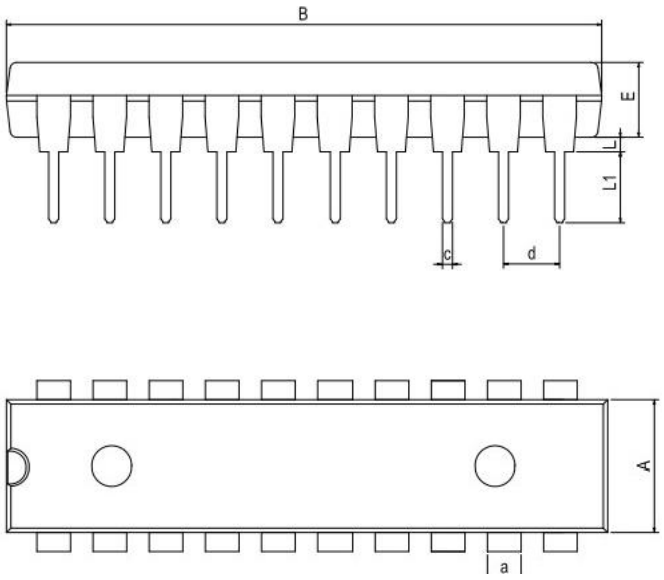
Type	Input		Output		
	V_1	VM	VM	Vx	Vγ
74HC374	GND to Vco	0.5×Vcc	0.5×Vcc	0.1×Vcc	0.9×Vcc
74HCT374	GND to 3V	1.3V	1.3V	0.1×Vcc	0.9×Vcc

Test Data

Type	Input		Load		S1 position		
	V_1	tr,t	CL	RL	tpHL,tpLH	tpzh,tpHz	toz tpu
74HC374	GND to Vcc	6ns	15pF,50pF	1kΩ	open	GND	Vcc
74HCT374	GND to 3V	6ns	15pF,50pF	1kΩ	open	GND	Vcc

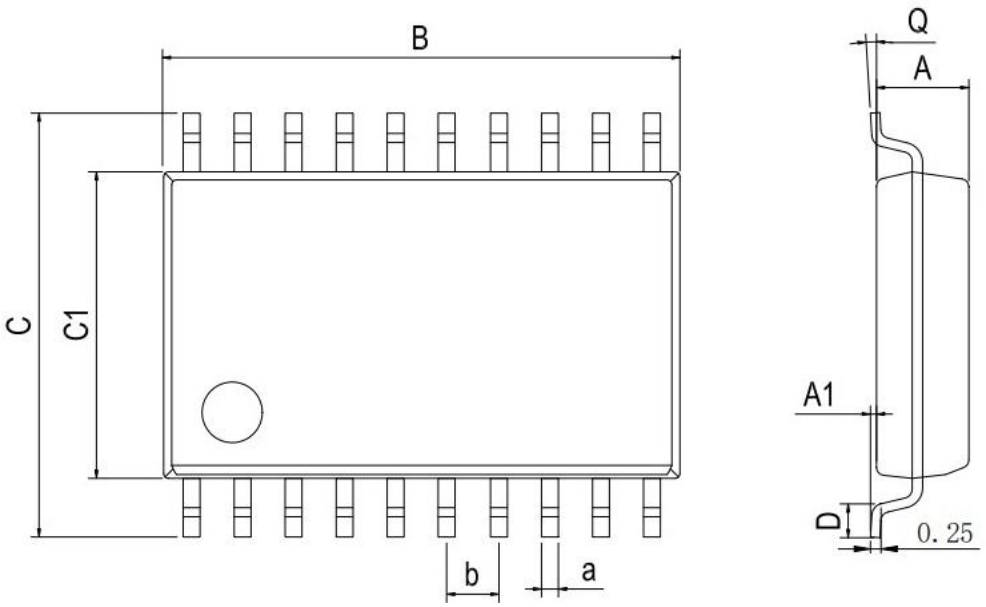
Physical Dimensions

DIP-20



Dimensions In Millimeters(DIP-20)										
Symbol:	A	B	D	D1	E	L	**L1**	**a**	**C**	**d**
Min:	6.10	24.95	8.10	7.42	3.10	0.50	**3.00**	**1.50**	**0.40**	**2.54 BSC**
Max:	6.68	26.55	10.9	7.82	3.55	0.70	**3.60**	**1.55**	**0.50**	

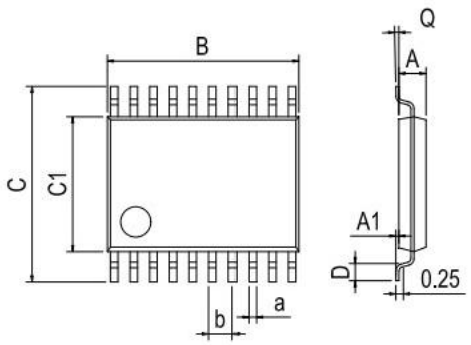
SOP-20



Dimensions In Millimeters(SOP-20)									
Symbol:	**A**	**A1**	B	C	**C1**	**D**	**Q**	**a**	**b**
Min:	2.10	0.05	12.50	10.21	**7.40**	**0.45**	**0°**	**0.35**	**1.27 BSC**
Max:	2.50	0.25	13.00	10.61	**7.60**	**1.25**	**8°**	**0.45**	

Physical Dimensions

TSSOP-20



Dimensions In Millimeters(TSSOP-20)									
Symbol:	**A**	**A1**	**B**	C	C1	**D**	**Q**	**a**	**b**
Min:	0.85	0.05	6.40	6.20	4.30	**0.40**	**0°**	**0.20**	**0.65 BSC**
Max:	1.05	0.20	6.60	6.60	**4.50**	**0.80**	**8°**	**0.25**	