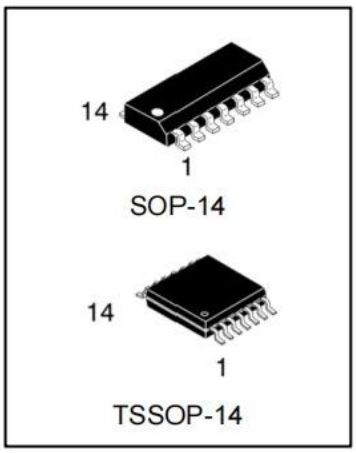
General Description

The 74HC74 is identical in pinout to the LS74.The device inputs are compatible with standard CMOS outputs;with pullup resistors,they are compatible with LSTTL outputs.

This device consists of two D flip-flops with individual Set,Reset,and Clock inputs.Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and Q outputs are available from each flip-flop.The Set and Reset inputs are asynchronous

Features

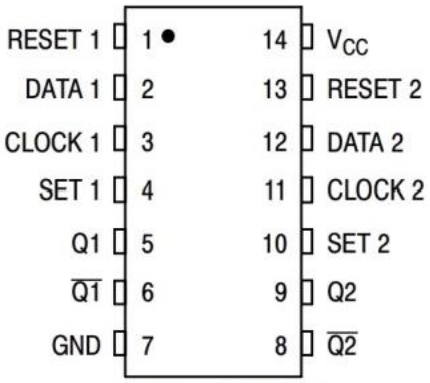
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7A Requirements
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 128 FETs or 32 Equivalent Gates
- Pb-Free Packages are Available



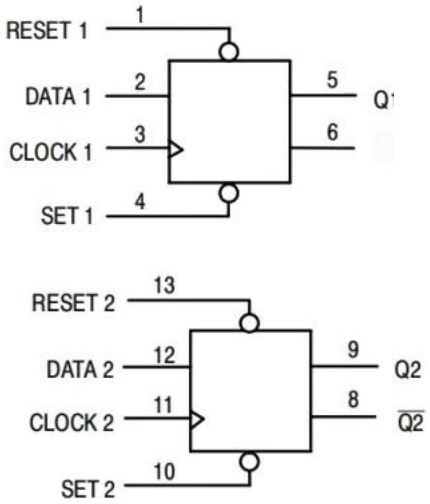
Order Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC74M/TR	SOP-14	74HC74	REEL	2500pcs/reel
74HC74MT/TR	TSSOP-14	HC74	REEL	2500pcs/reel

PIN ASSIGNMENT



LOGIC DIAGRAM



FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	Q
⊥	H	X	X	H	L
		X	X	L	H
L		X	X	H*	H*
H	H		H	H	L
⊥	H		L	No Change	
⊥	H		X	No Change	
⊥	H	H	X	No Change	
⊥	H		X		

*Both outputs will remain high as long as Set and Reset are low,but theoutput states are unpredictable if Set and Reset go high simultaneously.

MAXIMUM RATINGS

Symbol	Parametet	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	-0.5 to+7.0	V
Vin	DC Input Voltage (Referenced to GND)	-0.5 to VCC +0.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to VCC +0.5	V
Iin	DC Input Current,per Pin	20	mA
Iout	DC Output Current,per Pin	25	mA
Icc	DC Supply Current,VCc and GND Pins	50	mA
PD	Power Dissipation in Still Air, SOP Packaget TSSOP Packaget	 500 450	mW
Tstg	Storage Temperature	-65 to +150	℃
TL	Lead Temperature,1 mm from Case for 10 Seconds (SOP or TSSOP Package)	245	℃

This device contains protection circuitry to guard against damage due to high static voltages or electric fields.However, precautions must betaken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance cir-cuit.For proper operation,Vin and Vout should be constrained to the range GND≤(Vin or Vout)≤VCC.

Unused inputs must always be tied to an appropriate logic voltage level (e.g.,either GND or VCC).
Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device.Maximum Ratings are stress ratings only.Functional operation above the Recommended Operating Conditions is not implied.Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Derating —SOP Package:-7 mWPC from 65°to 125℃

TSSOP Package:-6.1 mW/C from 65°to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VCC	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
Vin,Vout	DC Input Voltage,Output Voltage (Referenced to GND)	0	VCC	V
TA	Operating Temperature,All Package Types	-40	+85	℃
tr,tf	Input Rise and Fall Time (Figures 1,2,3) VCC =2.0 V VCC=3.0 V VCC=4.5V VCC=6.0 V	0 0 0 0	1000 600 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	VCC (V)	Guaranteed Limit			Unit
				-40 to 25℃	≤85℃	≤125℃	
VIH	Minimum High-Level InputVoltage	Vout =0.1 V or VCC-0.1V Iout|≤20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
VIL	Maximum Low-Level InputVoltage	Vout =0.1 V or VCC-0.1V Iout|≤20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
VoH	Minimum High-Level OutputVoltage	Vin =VIH or VIL Ioutl≤20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		Vin =VIH or VIL Ioutl≤2.4 mA Ioutl≤4.0 mA Iout|≤5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
VOL	Maximum Low-Level OutputVoltage	Vin =VIH or VIL Iout|≤20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		Vin =VIH or VIL |Ioutl≤2.4 mA Ioutl≤4.0 mA Iout|≤5.2 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
Iin	Maximum Input Leakage Current	Vin =VCC or GND	6.0	0.1	1.0	1.0	μA
ICC	Maximum Quiescent Supply Current (per Package)	Vin =VCC or GNDIout =0 μA	6.0	2.0	20	80	μA

AC ELECTRICAL CHARACTERISTICS (CL=50 pF, Inputr=tf=6.0 ns)

Symbol	Parameter	VcC (V)	Guaranteed Limit			Unit
			-40 to 25°C	≤85°C	≤125°C	
fmax	Maximum Clock Frequency (50%Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
tPLH, tPHL	Maximum Propagation Delay,Clock to Q or Q (Figures 1 and 4)	2.0 3.0 4.5 6.0	100 75 20 17	125 90 25 21	150 120 30 26	ns
tPLH, tPHL	Maximum Propagation Delay,Set or Reset to Q or Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	105 80 21 18	130 95 26 22	160 130 32 27	ns
tTLH, tTHL	Maximum Output Transition Time,Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
Cin	Maximum Input Capacitance		10	10	10	pF
CPD	Power Dissipation Capacitance (Per Flip-Flop)*	Typical @25°C,VCC =5.0 V 32				pF

*Used to determine the no-load dynamic power consumption:PD =CPD VCC2f+ICC VCC.

TIMING REQUIREMENTS (nputtr=tf=6.0 ns

Symbol	Parameter	VCC (V)	Guaranteed Limit			Unit
			-40 to 25°C	≤85°C	≤125°C	
tsu	Minimum Setup Time,Data to Clock (Figure 3)	2.0 3.0 4.5 6.0	80 35 16 14	100 45 20 17	120 55 24 20	ns
th	Minimum Hold Time,Clock to Data (Figure 3)	2.0 3.0 4.5 6.0	3.0 3.0 3.0 3.0	3.0 3.0 3.0 3.0	3.0 3.0 3.0 3.0	ns
trec	Minimum Recovery Time,Set or Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	8.0 8.0 8.0 8.0	8.0 8.0 8.0 8.0	8.0 8.0 8.0 8.0	ns
tw	Minimum Pulse Width,Clock (Figure 1)	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
tw	Minimum Pulse Width,Set or Reset (Figure 2)	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
tr,tf	Maximum Input Rise and Fall Times (Figures 1,2,3)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

SWITCHING WAVEFORMS

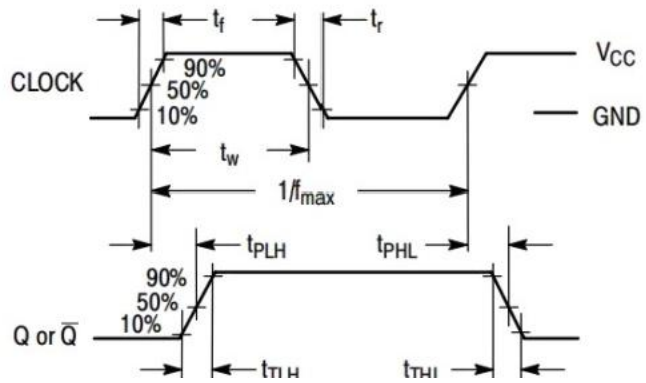


Figure 1.

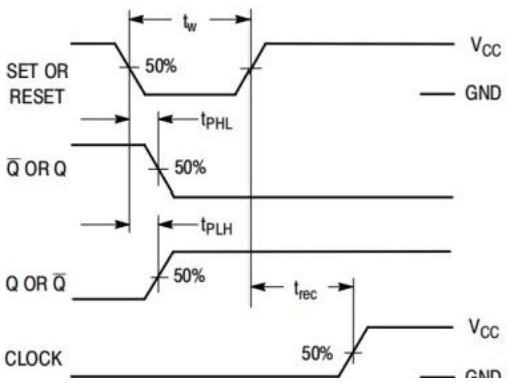


Figure 2.

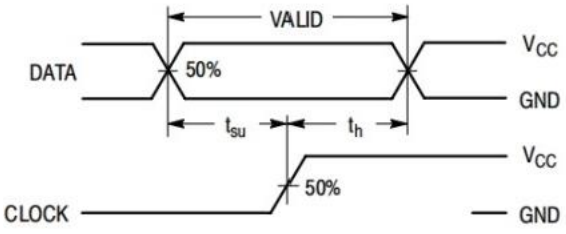
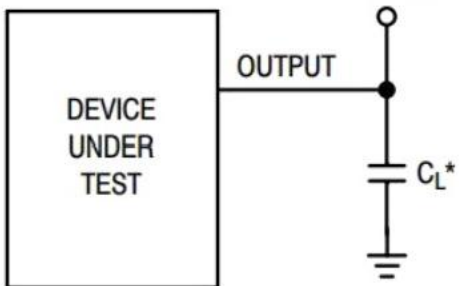


Figure 3.

TEST POINT



*Includes all probe and jig capacitance

Figure 4.

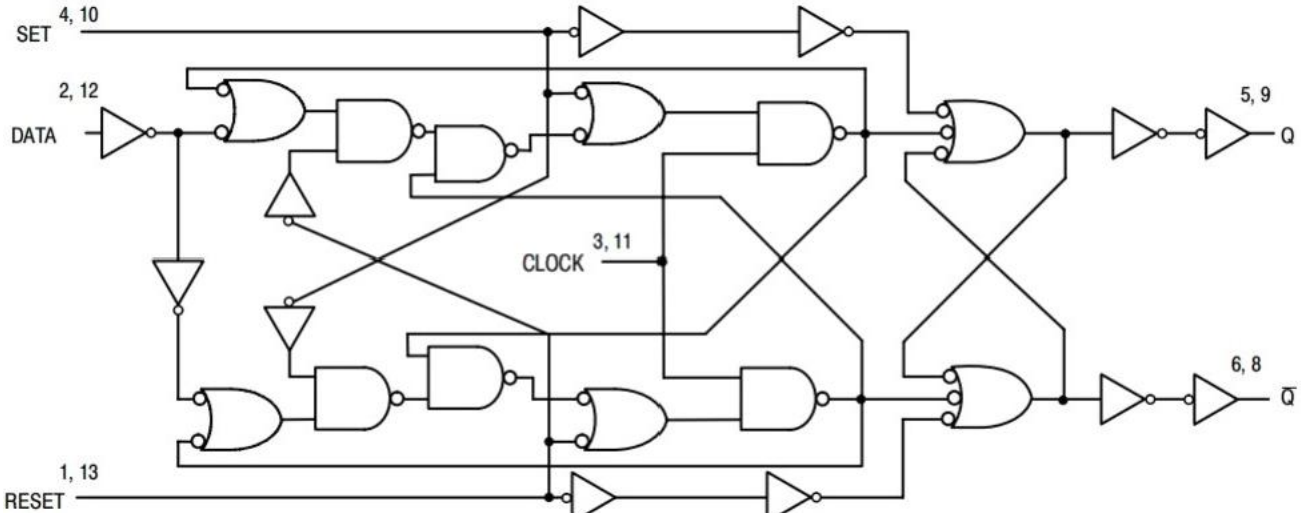
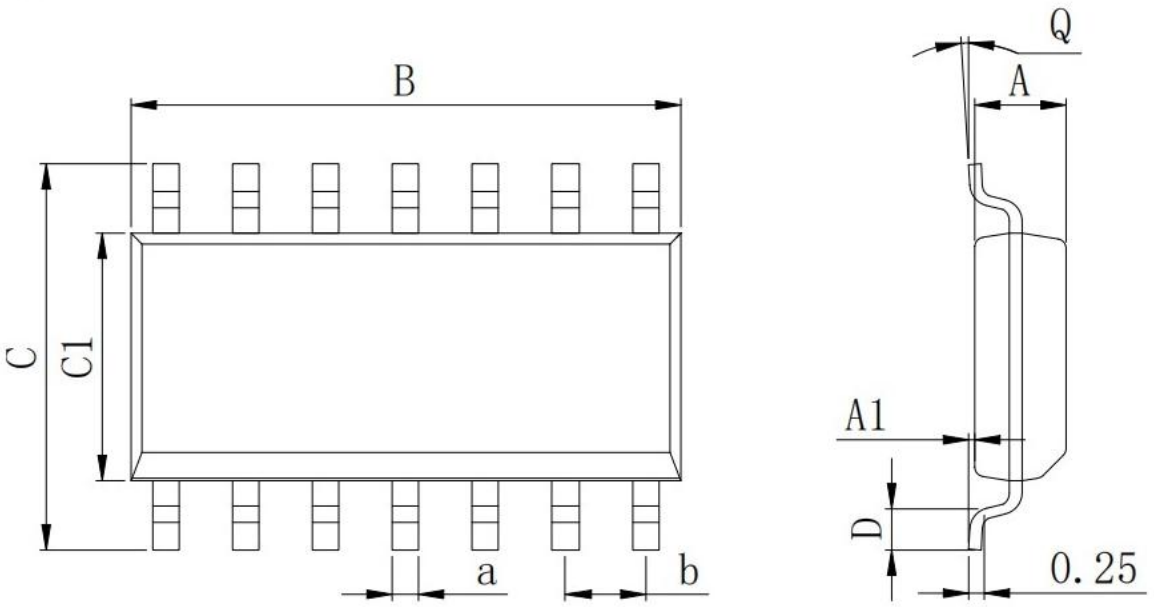


Figure 5.EXPANDED LOGIC DIAGRAM

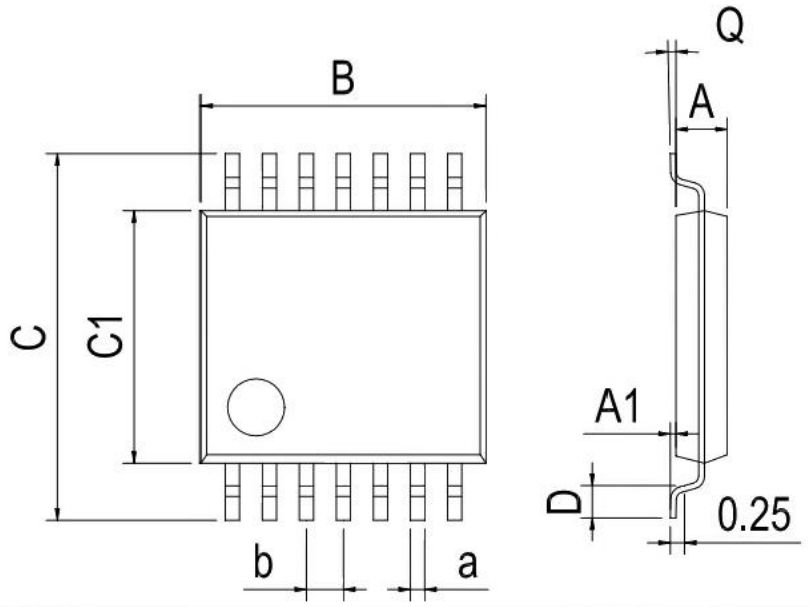
PHYSICAL DIMENSIONS

SOP-14



Dimensions In Millimeters(SOP-14)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	1.35	0.05	**8.55**	**5.80**	**3.80**	**0.40**	**0°**	**0.35**	**1.27 BSC**
Max	1.55	0.20	**8.75**	**6.20**	**4.00**	**0.80**	**8°**	**0.45**	

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	**A**	**A1**	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	