General Description

TThe CD4017 isa5 -stage Johnson decade counter with ten spike-free decoded active HIGH outputs(Q0 to Q9),an active LOW carry output from the most significant flip-flop(Q5—-9),active HIGH and active LOW clock inputs(CP0,—CP¹)and an overriding asynchronous master reset input(MR).

The counter is advanced by either a LOW-to-HIGH transition at CPO while Pl is LOW or a HIGH-to-LOW transition at CP1 while CPO is HIGH.

When cascading counters,the Q5-9 output,which is LOW while the counter is in states 5,6,7,8,and 9,can be used to drive the CPO input of the next counter. A HIGH on MR resets the counter to zero(Q0=Q-5-9=HIGH;Q1 to Q9=LOW)independent of the clock inputs(CP0,CP1).

Automatic counter code correction is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

It operates over a recommended VDD power supply range of 3 V to 15 Vreferenced to VSS(usually ground). Unused inputs must be connected to VDD,VSS,or another input.

Features

- Wide supply voltage range from 3V to 15V
- Automatic counter correction
- Tolerant of slow clock rise and fall times
- 5V,10V,and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40℃ to +85℃
- Packaging information:DIP16/SOP16/TSSOP16

Order Information

DEVICE	Package Type	MARKING	Packing	Packing QTY
CD4017BE/CD4017BN	DIP-16	CD4017B	TUBE	2000/box
CD4017BM/TR	SOP-16	CD4017B	REEL	2500/reel
CD4017BMT/TR	TSSOP-16	CD4017B	REEL	2500/reel

2.Block Diagram And Pin Description

2.1 、Block Diagram

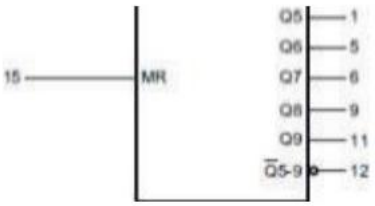


Figure 1.Logic symbol

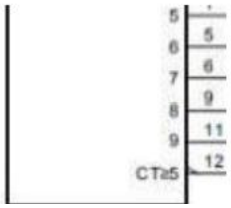


Figure 2 IEE logic symbol

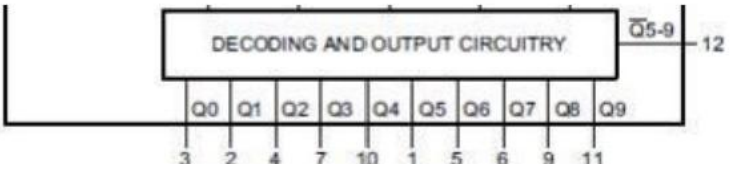


Figure 3 . Functional diagram

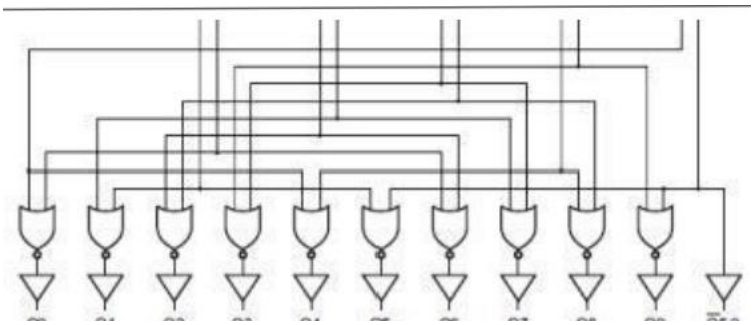


Figure 4. Logic diagram

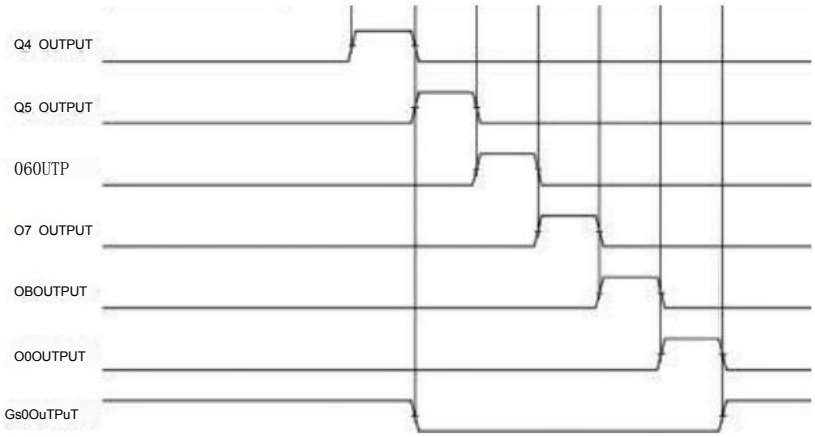
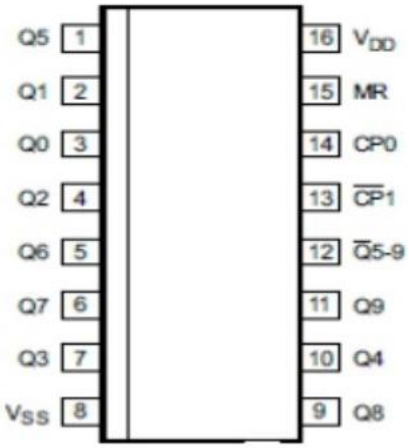


Figure 5. Timing diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No	Pin Name	Description
1	Q5	decoded output
2	Q1	decoded output
3	Q0	decoded output
4	Q2	decoded output
5	Q6	decoded output
6	Q7	decoded output
7	Q3	decoded output
8	Vss	ground(0 V)
9	Q8	decoded output
10	Q4	decoded output
11	Q9	decoded output
12	Q5-9	carry output(active LOW)
13	CP1	clock input(HIGH-to-LOW edge-triggered)
14	CP0	clock input(LOW-to-HIGH edge-triggered)
15	MR	master reset input
16	VDD	supply voltage

2.4、Function Table

Input			Operation
MR	CP0	CP1	
H	X	X	Q0=Q5-9=H;Q1 toQ9=L
L	H	↓	counter advances
L	1	L	counter advances
L	L	X	no change
L	X	H	no change
L	H		no change
L	↓	L	no change

Note:H=HIGH voltage level;L=LOW voltage level;X=don't care,

↑=positive-going transition; ↓=negative-going transition.

3 Electrical Parameter

3.1、 Absolute Maximum Ratings

(Voltages are referenced to Vss(ground=0 V),unless otherwise specified.)

Paramet er	Symbol	Condition s		Min.	Max.	Unit
supply voltage	VDD			-05	+18	V
DC input current	Iik	any one input			±10	mA
input voltage	Vi	all inputs		-05	VDD+05	V
storage temperature	Tstg			-65	+150	℃
total power dissipation	Ptot				500	mW
device dissipation	P	per output transistor			100	mW
Soldering temperature	TL	10s	DIP	245		℃
			SOP	250		

Note:

[1]For DIP16 packages:above 70℃ the value of Piot derates linearly with 12 mW/K.

[2]For SOP¹6 packages: above 70℃ the value of Pot derates linearly with 8mW/K.

[3]For(T)SSOP16 packages:above 60℃ the value of Pot derates linearly with 5.5mW/K.

3.2、 Recommended Operating Conditions

Paramet er	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	VDD		3		15	V
ambient t emperature	Tamb	in free air	-40		+85	℃
clock input frequency	fcl	VDD=5V			2.5	MHz
		VDD=10V	_	_	5	MHz
		Vpd=15V			5.5	MHz
clock pulse width	tw	VDd=5 V	200			nS
		VDD=10V	90			nS
		VDD=15V	60			nS
clock rise and fall time	trcl,tfcl	VDp=5 V	unlimited			
		VDD=10V				
		VDD=15V				
clock inhibit setup time	t_s	VDd=5 V	230			nS
		VDD=10V	100			nS
		VDD=15V	70			ns
reset pulse width	tgw	VDp=5 V	260			nS
		Vdp=10V	110			ns
		VDD=15V	60			nS
reset removal time	tree	VDp=5 V	400			nS
		VDD=10V	280			ns
		VDD=15V	150			ns

			0, 15	15		0.05		0.05	V
HIGH-level output voltage	Voh		0, 5	5	4.95		4.95		V
			0, 10	10	9.95		9.95		V
			0, 15	15	14.95		14.95		V
LOW-level input voltage	V μ	0.5, 4.5		5		1.5		1.5	V
		1, 9		10		3		3	V
		1.5, 13.5		15		4		4	V
HIGH-leve input voltage	ViH	0.5, 4.5		5	3.5		3.5		V
		1, 9		10	7		7		V
		1.5, 13.5		15	11		11		V
input leakage current	I_1		0, 15	15		±0.1		±1	uA

3.3.3、AC Characteristics

(Tamb=25℃, Vss=0V, tr, tr=20ns, CL=50pF, RL=200kQ, unless otherwise specified.)

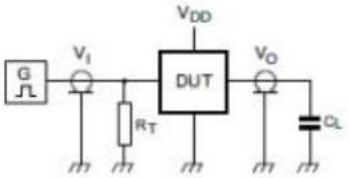
Parameter	Symbol	Conditions		Min.	Typ.	Max	Unit
propagation delay time	tpHL, tpLH	CP0, CP1 to Q0 to Q9; see Figure 7	Vdd=5V		325	650	ns
			VDp=10V		135	270	ns
			VDd=15V		85	170	ns
		CP₀, CP1 to Q5-9; see Figure 7	Vdd=5V		300	600	ns
			VDp=10V		125	250	ns
			Vdp=15V		80	160	ns
		MR to Q0 to Q9; see Figure 7	Vdp=5V		265	530	ns
			VDp=10V		115	230	ns
			VDD=15V		85	170	ns
transition time	tt	see Figure 7	Vdd=5V		100	200	ns
			VDp=10V		50	100	ns
			VDp=15V		40	80	ns
pulse width	tw	see Figure 8	Vpd=5V		100	200	ns
			VDp=10V		45	90	ns
			VDd=15V		30	60	ns
clock rise and fall time	tcl, ticl		VDD=5V	unlimited			
			VDp=10V				
			VDd=15V				
maximum clock frequency	fcl	see Figure 8	Vpd=5V	2.5	5		MHz
			VDp=10V	5	10		MHz
			VDp=15V	5.5	11		MHz
setup time	ts	CP0 to CPI see Figure 9	Vpd=5V		115	230	ns
			VDp=10V		50	100	ns
			VDp=15V		35	70	ns
reset remova time	trec	MR input; see Figure 8	Vpd=5V		200	400	ns
			VDp=10V		140	280	ns
			VDp=15V		75	150	ns
input capacitance	Ci	any input			5		pF

Note:tt is the same as trlh and trhl

4、Testing Circuit

4.1、AC Testing Circuit

a.Input wavefoms



b.Test circuit

Figure 6.Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

CL=Load capacitance including jig and probe capacitance.

Rr=Termination resistance should be equal to the output impedance Zo of the pulse generator.

4.2、AC Testing Waveforms

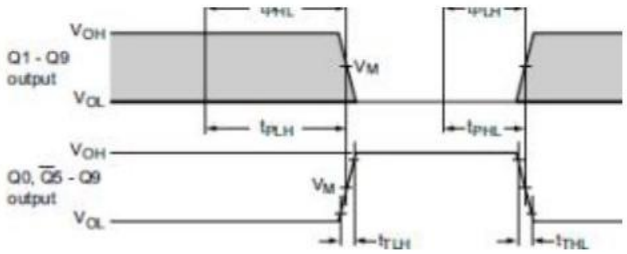


Figure 7.Waveforms showing the propagation delays for CP0,CP¹to Qn,Q5-9 outputs and the output transition times.

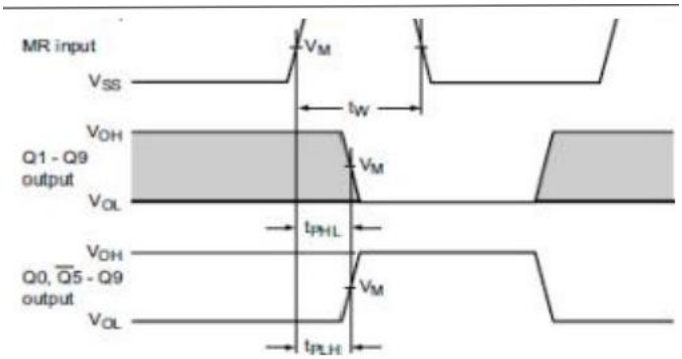


Figure 8.Waveforms showing the minimum pulse width for CP0,CP¹and MR input;the maximum

frequency for CPO and CP¹input,the recovery time for MR and the MR input to Qn and Q5-9 output propagation dela

Figure 9.Waveforms showing hold times for CPO to CPl and CP1 to CPO

4.3 、Measurement Points

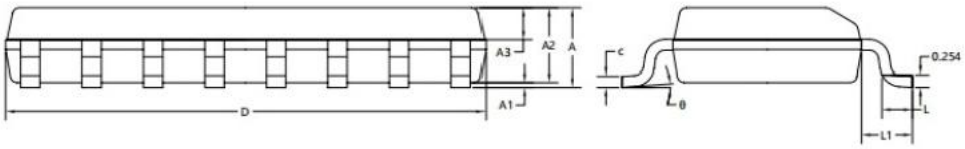
Supply voltage	Input	Output
VDD	VM	VM
5V to 15V	0.5×VDD	05×VDD

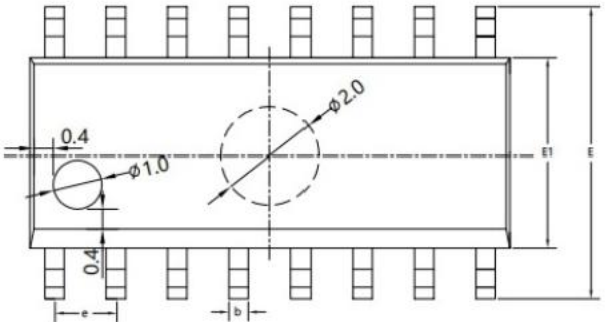
4.4 、Test Data

Supply voltage	Input		Load
VDD	VI	tr,tr	CL
5V to 15V	Vss or VDD	⩽20ns	50pF

5 、Package Information

5.1、DIP16

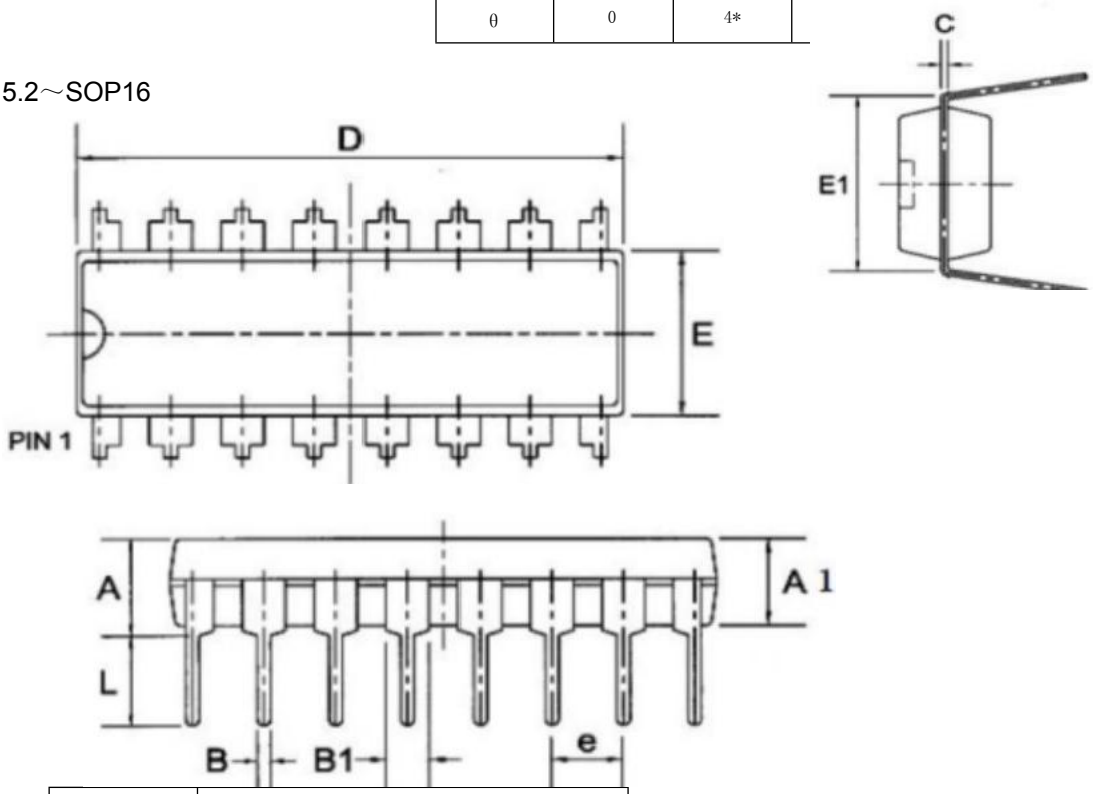




SYMBOL	MILUMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	065	0.70
b	0.30	040	0.50
c	0.15	020	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	060	0.70

L1	1.05BSC		
θ	0	4*	

5.2～SOP16



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A			4.31
A1	3.15	3.30	3.65
B		0.50	
B1		1.6	
C		0.27	
D	19.00	19.20	19.60
E	6.20	6.50	6.60
E1		8.0	
e		2.3	
L	3.00	3.20	3.60