

General Description

The CD4027 is a edge-triggered dual JK flip-flop which features independent set-direct (SD),clear-direct (CD),clock (CP)inputs and outputs(Q,Q).Data is accepted when CP is LOW,and transferred to the output on the positive-going edge of the clock.The active HIGH asynchronous clear-direct (CD)and set-direct (SD)inputs are independent and override the J,K,and CP inputs.The outputs are buffered for best system performance.

It operates over a recommended VDD power supply range of 3V to 15V referenced to VSS (usually ground). Unused inputs must be connected to VDD,VSS,or another input.

Features

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V,10V,and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from-40C to+105C
- Packaging information:DIP16/SOP16/TSSOP16

Order Information

DEVICE	Package Type	MARKING	Packing	Packing QTY

2. Block Diagram And Pin Description

2.1 、 Block Diagram

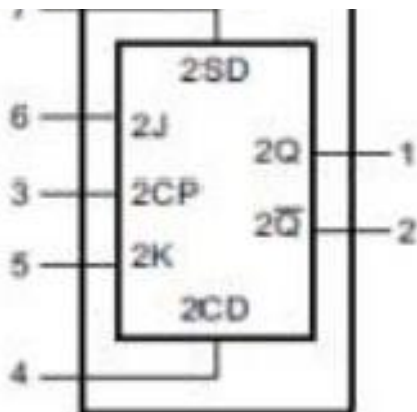


Figure 1. Functional diagram

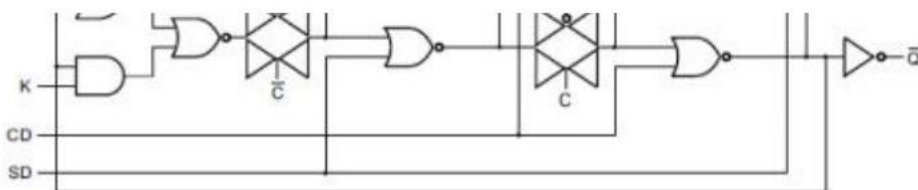
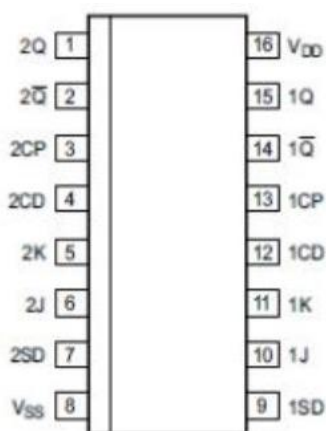


Figure 2. Logic diagram (one gate)

2.2 、 Pin Configurations



2.3、 Pin Description

Pin No.	Pin Name	Description
	2Q	true output
2	2Q	complement output
3	2CP	clock input (LOW-to-HIGH edge-triggered)
4	2CD	asynchronous clear-direct input (active HIGH)
5	2K	synchronous input
6	2J	synchronous input
7	2SD	asynchronous set-direct input (active HIGH)
8	V _{SS}	ground(0 V
9	1SD	asynchronous set-direct input (active HIGH)
10	1J	synchronous input
11	1K	synchronous input
12	1CD	asynchronous clear-direct input (active HIGH)
13	1CP	clock input (LOW-to-HIGH edge-triggered)
14	1Q	complement output
15	1Q	true output
16	V _{DD}	supply voltage

2.4、 Function Table

Input					Output	
nSD	nCD	nCP	nJ	nK	nQ	nQ
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H
L	L	↑	L	L	10 change	no change
L	L		H	L	H	L
L	L		L	H	L	H
L	L		H	H	nQ	nQ

Note:H=HIGH voltage level;L=LOW voltage level;X=don't care;↑=LOW-to-HIGH clock transition.

3 Electrical Parameter

3.1 Absolute Maximum Ratings

(Voltages are referenced to Vss(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Max	Unit
supply voltage	VDD		-0.5	+18	V
DC input current	I _k	any one input		±10	mA
input voltage	V _i	all inputs	-0.5	V _{Dd} +0.5	V
storage temperature	T _{sg}		-65	+150	°C
total power dissipation	P _{tot}			500	mW
device dissipation	P	per output transistor		100	mW
Soldering temperature	TL	10s	DIP	245	°C
			SOP	250	°C

Note:

[1] For DIP16 packages: above 70°C the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP16 packages: above 70°C the value of P_w derates linearly with 8mW/K.

[3] For (T)SSOP16 packages: above 60°C the value of P_a derates linearly with 5.5mW/K.

3.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
supply voltage	V _{pp}		3		15	V
ambient temperature	T _{amb}	in free air	-40		+105	°C
clock pulse width	tw _{cl}	V _{dp} =5 V	140			ns
		V _{dp} =10V	60			ns
		V _{pp} =15V	40			ns
clock rise and fall time	t _{cl} , t _{icl}	V _{dp} =5 V			45	µs
		V _{dp} =10V			5	µs
		V _{dp} =15V			2	µs
clock input frequency	f _{cl}	V _{dp} =5 V	DC		35	MHz
		V _{dp} =10V		8	MHz	
		V _{dp} =15V		12	MHz	
set-up time	t _s	V _{Dd} =5 V	200			ns
		V _{dp} =10V	75			ns
		V _{dp} =15V	50			ns
set or reset pulse width	t _{ws}	V _{pp} =5 V	180			ns
		V _{pp} =10V	80			ns
		V _{pp} =15V	50			ns

3.3 Electrical Characteristics

3.3.1 DC Characteristics 1

(Tamb=25 C, voltages are referenced to Vss (ground=0 V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			Tamb=25C			Unit
		Vo	ViN	VDD	Min.	Typ.	Max.	
supply current	Ibp		0, 5	5		0.02	1	uA
			0, 10	10		0.02	2	uA
			0, 15	15		0.02	4	uA
LOW-level output current	Iol	0.4	0, 5	5	0.51	1		mA
		0.5	0, 10	10	1.3	2.6		mA
		1.5	0, 15	15	3.4	6.8		mA
HIGH-level output current	Ioh	4.6	0, 5	5	-0.51	-1		mA
		2.5	0, 5	5	-1.6	-3.2		mA
		9.5	0, 10	10	-1.3	-2.6		mA
		13.5	0, 15	15	-3.4	-6.8		mA
LOW-level output voltage	Vol		0, 5	5		0	0.05	V
			0, 10	10		0	0.05	V
			0, 15	15		0	0.05	V
HIGH-level output voltage	VoH		0, 5	5	4.95	5		V
			0, 10	10	9.95	10		V
			0, 15	15	14.95	15		V
LOW-level input voltage	Vn	0.5, 4.5		5			1.5	V
		1, 9		10			3	V
		1.5, 13.5		15			4	V
HIGH-level input voltage	VH	0.5, 4.5		5	3.5			V
		1, 9		10	7			V
		1.5, 13.5		15	11			V
input leakage current	Ii		0, 15	15		±10 ⁵	±0.1	uA

3.3.2、DC Characteristics 2

(Tamb=-40 C to+105 C, voltages are referenced to Vss(ground=0 V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			Tamb=-40C		Tamb=+85C		Tamb=+105C		Unit
		Vo	ViN	VpD	Min.	Max.	Min.	Max.	Min	Max	
supply current	IpD		0, 5	5		1		30		30	uA
			0, 10	10		2		60		60	uA
			0, 15	15		4		120		120	uA
LOW-level output current	lor	0. 4	0, 5	5	0. 61		0. 42		0. 36		mA
		0. 5	0, 10	10	1. 5		1. 1		0. 9		mA
		1. 5	0, 15	15	4		2. 8		2. 4		mA
HIGH-level output current	loh	4. 6	0, 5	5	-0. 61		-0. 42		-0. 36		mA
		2. 5	0, 5	5	-1. 8		-1. 3		-1. 15		mA
		9. 5	0, 10	10	-1. 5		-1. 1		-0. 9		mA
		13. 5	0, 15	15	-4		-2. 8		-2. 4		mA
LOW-level output voltage	Vol		0, 5	5		0. 05		0. 05	—	0. 05	V
			0, 10	10		0. 05		0. 05		0. 05	V
			0, 15	15		0. 05		0. 05		0. 05	V
HIGH-level output voltage	VoH		0, 5	5	4. 95		4. 95		4. 95		V
			0, 10	10	9. 95		9. 95		9. 95		V
			0, 15	15	14. 95		14. 95		14. 95		V
LOW-level input voltage	Vn	0. 5, 4. 5		5		1. 5		1. 5		1. 5	V
		1, 9		10		3		3		3	V
		1. 5, 13. 5		15		4		4		4	V
HIGH-level input voltage	VH	0. 5, 4. 5		5	3. 5		3. 5		3. 5		V
		1, 9		10	7		7		7		V
		1. 5, 13. 5		15	11		11		11		V
input leakage current	I _I		0, 15	15		±0. 1		±1		±1	uA

4、Testing Circuit

4.1、AC Testing Circuit

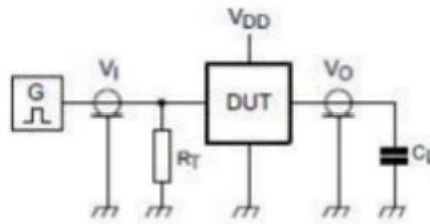


Figure 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_1 =Load capacitance including jig and probe capacitance.

R_1 =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

4.2、AC Testing Waveforms

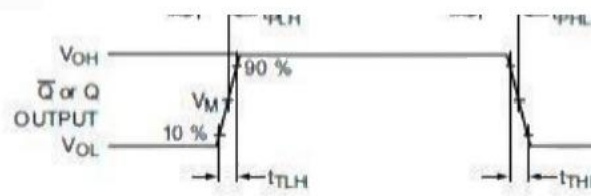


Figure 4. Waveforms showing rise, fall and transition times and propagation delays

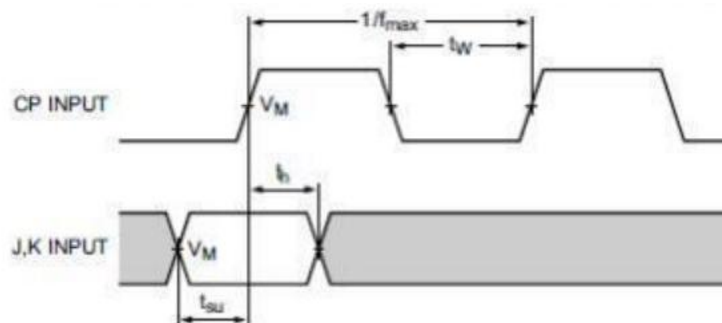


Figure 5. Waveforms showing set-up and hold times and minimum clock pulse width

Figure 6. Waveforms showing pulse widths

4.3、 Measurement points

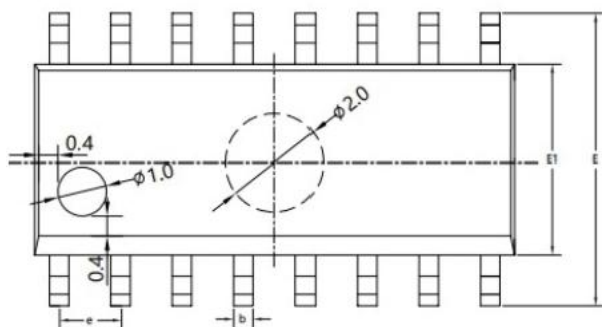
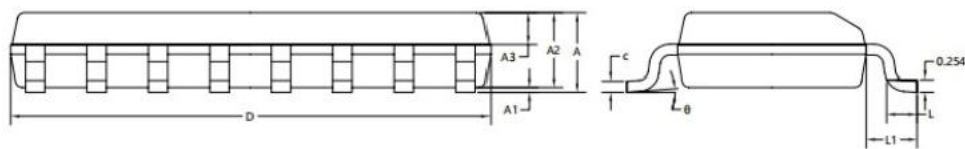
Supply voltage	Input	Output
V _{dp}	V _M	V _M
5V to 15V	0.5×V _{oo}	0.5×V _{DD}

4.4、 Test data

Supply voltage	Input		Load
V _{pD}	V _i	t _r , t _r	C _L
5V to 15V	V _{ss} or V _{pD}	≤20ns	50pF

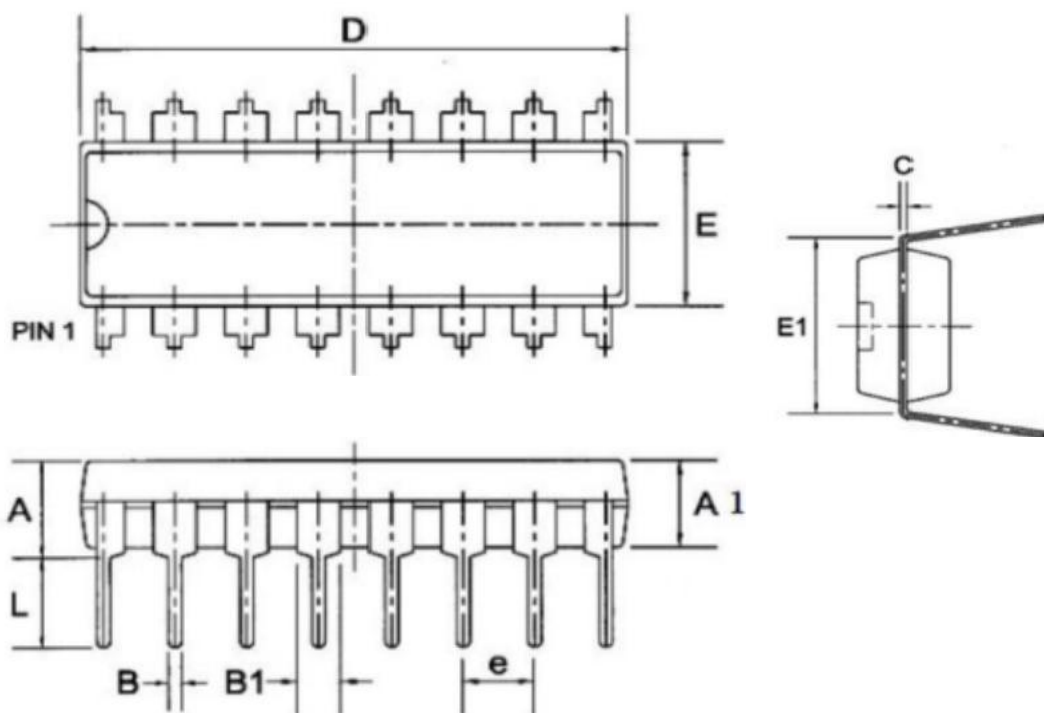
5、 Package Information

5.1、 DIP16



SYMBOL	MILUMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.0585C		
theta	sigma	4*	8*

5.2~SOP16



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	--	=	4.31
A1	3.15	3.30	3.65
B	-	0.50	-
B1	--	1.6	--
C	-	0.27	
D	19.00	19.20	19.60
E	6.20	6.50	6.60
E1		8.0	
e	--	2.3	--
L	3.00	3.20	3.60