General Description

The SN75LBC184 and SN65LBC184 are differ-ential data line transceivers in the trade-standard footprint of the SN75176 with built-in protection against high-energy noise transients.This feature provides a substantial increase in reliability for better immunity to noise transients coupled to the data cable over most existing devices.Use of these circuits provides a reliable low-cost direct-coupled (with no isolation transfomer) data line interface without requiring any external components.

The SN75LBC184 and SN65LBC184 can with-stand overvoltage transients of 400-W peak (typical). The conventional combination wave called out in IEC 61000-4-5 simulates the overvoltage transient and models a unidirectional surge caused by overvoltages from switching and secondary lightning transients.

A biexponential function defined by separate rise and fall times for voltage and current simulates the combination wave.The standard 1.2 μs/50μs combination waveform is shown in Figure 1 and in the test description in Figure 15.

The device also includes additional desirable features for party-linedata buses in electrically noisy environment applications including industrial process control.The differential-driver design incorporates slew-rate-controlled outputs sufficient to transmit data up to 250 kbps.Slew-rate control allows longer unterminated cable runs and longer stub lengths from the main backbone than possible with uncontrolled and faster voltage transitions.A unique receiver design provides a fail-safe output of a high level when the inputs are left floating(open circuit).The SN75LBC184 and SN65LBC184 receiver also includes a high input resistance equivalent to one-fourth unit load allowing connection of up to 128 similar devices on the bus.

The SN75LBC184 is characterized for operation from 0℃ to 70℃.The SN65LBC184 is characterized from-40℃to 85℃.

FEATURES

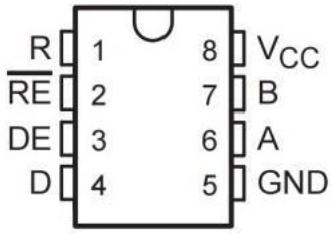
- Integrated Transient Voltage Suppression
- ESD Protection for Bus Terminals Exceeds:
  ±30 kV IEC 61000-4-2,Contact Discharge
  ±15 kV IEC 61000-4-2,Air-Gap Discharge
  ±15 kV EIA/JEDEC Human Body Model
- Circuit Damage Protection of 400-W Peak (Typical)Per IEC 61000-4-5
- Controlled Driver Output-Voltage Slew Rates Allow Longer Cable Stub Lengths
- 250-kbps in Electrically Noisy Environments Open-Circuit Fail-Safe Receiver Design
- 1/4 Unit Load Allows for 128Devices Connected on Bus
- Thermal Shutdown Protection
- Power-Up/-Down Glitch Protection
- Each Transceiver Meets or Exceeds the Requirements of TIA/ElA-485 (RS-485)and ISO/IEC 8482:1993(E)Standards
- Low Disabled Supply Current 300 μA Max
- Pin Compatible With SN75176
- Applications:
  - Industrial Networks
  - Utility Meters
  - Motor Contro

ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
SN65LBC184N	DIP-8	65LBC18	TUBE	2000pcs/box
SN65LBC184M/TR	SOP-8	6LB184	REEL	2500pcs/reel
SN65LBC184MM/TR	MSOP-8	6LB184	REEL	3000pcs/reel
SN75LBC184N	DIP-8	75LBC184	TUBE	2000pcs/box
SN75LBC184M/TR	SOP-8	7LB184	REEL	2500pcs/reel
SN75LBC184MM/TR	MSOP-8	7LB184	REEL	3000pcs/reel

Pin Configuration

DIP-8/SOP-8/MSOP-8



FUNCTIONAL LOGIC DIAGRAM(POSITIVE LOGIC)

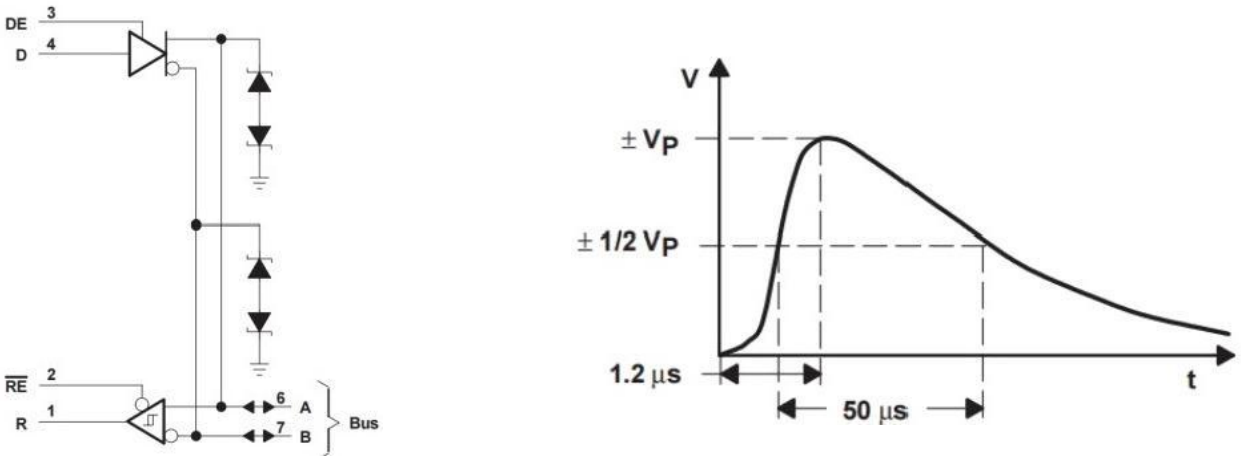
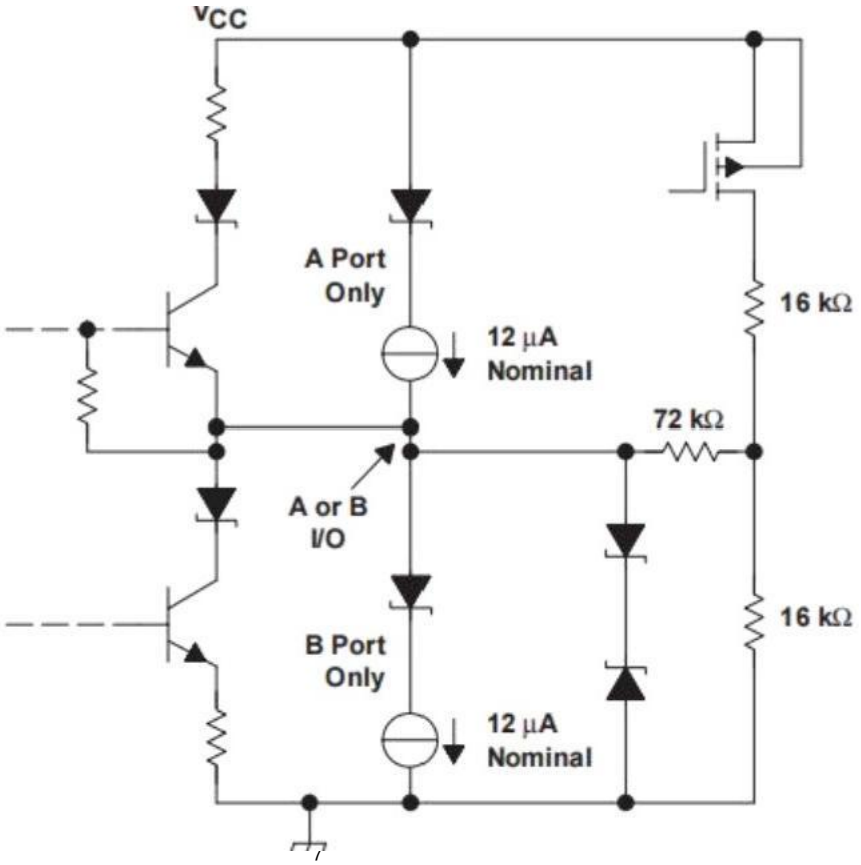


Figure 1.Surge Waveform —Combination Wave

SCHEMATIC OF INPUTS AND OUTPUTS



DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

H=high level,L=low level,?=indeterminate,
X=irrelevant,Z =high impedance (off)

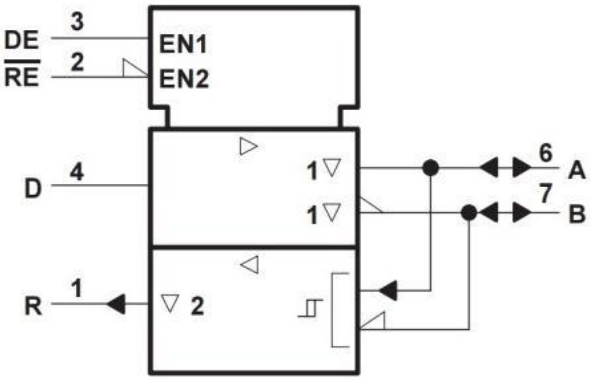
RECEIVER FUNCTION TABLE

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A-B	RE	R
VID≥0.2V	L	H
-0.2V<VID<0.2V	L	?
VID≤-0.2V	L	L
X	H	Z
Open	L	H

H=high level,L=low level,?=indeterminate,

X=irrelevant,Z =high impedance (off)

LOGIC SYMBOL



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)'″

Condition	Min	Max
Supply voltage,VCC(see Note 1)	-0.5V	7V
Continuous voltage range at any bus terminal	-15V	15V
Data input/output voltage	-0.3	7
Receiver output current,IO	-20mA	+20mA
Electrostatic discharge		
Contact discharge(IEC61000-4-2)A,B,ND(see Note 2)		30KV
Air discharge(IEC61000-4-2) A,B,ND(see Note 2)		15KV
Human body model(see Note 3)A,B,ND(see Note 2)		15KV
All pins		3KV
All terminals(Class 3A)(see Note 2)		8KV
All terminals(Class 3A)(see Note 2)		1200V
Continuous total power dissipatiom(see Note 4)	Internally Limited	
Lead Temperature (Soldering,10 seconds)	245°	

(1)Stresses beyond those listed under "absolute maximum ratings"may cause permanent damage to the device.These are stress ratings only,and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions"is not implied.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:

1. All voltage values,except differential input/output bus voltage,are with respect to network ground terminal.
2. GND and bus terminal ESD protection is beyond readily available test equipment capabilities for IEC 61000-4-2,EIAJEDEC test method A114-A and MIL-STD-883C method 3015.Ratings listed are limits of test equipment;device performance exceeds these limits.
3. Tested in accordance with JEDEC Standard 22,Test Method A114A.
4. The drivershuts down at a junction temperature of approximately 160℃.To operate below this temperature,see the Dissipation Rating Table.

DISSIPATION RATING TABLE

PACKAGE	TA≤25℃ POWER RATING	DERATING FACTOR ABOVE TA=25℃	TA=70°℃ POWER RATING	TA=85℃ POWER RATING
N M	725 mW 1150 mW	**5.8 mW/℃** **9.2 mW/℃**	**464 mW** **736 mW**	**377 mW** **598 mW**

recommended operating conditions

		MIN(2)	TYP	MAX	UNIT
Supply voltage,Vcc		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode),VI or VIC		-7		12	V
High-level input voltage,VIH	D,DE,and RE	2			V
Low-level input voltage,VIL	D,DE,and RE			0.8	V
Differential input voltage,IVID				12	V
High-level output current,IOH	Driver	-60			mA
	Receiver	-8			mA
Low-level output current,IOL	Driver			60	mA
	Receiver			4	
Operating free-air temperature,TA	SN75LBC184	0		70	℃
	SN65LBC184	-40		85	℃

(2) The algebraic convention,in which the less-positive (more-negative)limit is designated minimum,is used in this data sheet.

DRIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	ALTERNATE SYMBOLS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
cc Supply current	NA	DE=RE =5 V,No Load		12	25	mA
		DE=0V,RE =5V, No Load		175	300	μA
IH High-level input current (D,DE,RE)	NA	VI=2.4 V			50	μA
L Low-level input current (D,DE,RE)	NA	Vi=0.4V	-50			μA
Short-circuit output current los (see Note 5)	NA	Vo=-7V	-250	-120		mA
		Vo=VCC			250	
		Vo=12 V			250	
loz High-impedance output current	NA		See Receiver I			mA
Vo Output voltage	Voa,Vot	Io=0	0		VCC	V
VoC(PP Peak-to-peak change in common-mode output voltage during state transitions	NA	See Figures 5 and 6		0.8		V
Voc Common-mode output voltage	|Vosl	See Figure 4	1		3	V
mode △VoC(Ss)l Magnitude of change,common-steady-state output voltage	Vos -Vos	See Figure 5			0.1	V
IVoDI Magnitude of differential outputvoltage	Vo	Io=0	1.5		6	V
IVA-VBI		RL=54Q,See Figure 4	1.5			V
△IVODI Change in differential voltage mag-nitude between logic states	IIVtl —|Vtll	RL=54Ω			0.1	V

All typical values are measured with TA=25°C and VCC =5 V.

NOTE 5:This parameter is measured with only one output being driven at a time.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
td(DH)Differential output delay time,low-to-high-level output	RL=54Ω,CL=50 pF See Figure 5			1.3	μs
td(DL)Differential-output delay time,high-to-low-level output				1.3	μs
tPLH Propagation delay time,low-to-high-level output			0.5	1.3	μs
tPHL Propagation delay time,high-to-low-level output			0.5	1.3	μs
tsk(p Pulse skew(ltd(DH)-dt (DL)l)			75	150	ns
tr Rise time,single ended		0.25		1.2	μs
tf Fall time,single ended		0.25		1.2	μs
tpZH Output enable time to high level	RL=110Ω See Figure 2			3.5	μs
tpZL Output enable time to low level	RL=110Ω See Figure 3			3.5	μs
tPHZ Output disable time from high level	RL=110Ω See Figure 2			2	μs
tPLZ Output disable time from low level	RL=110Ω See Figure 3			2	μs

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

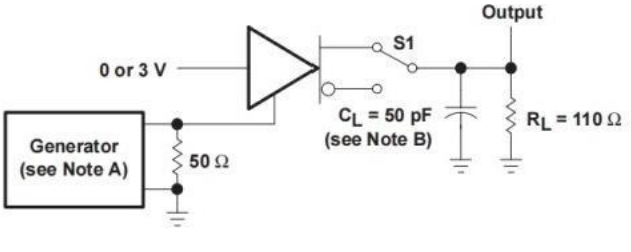
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Icc Supply current (total package)	DE=RE =0 V,No Load				3.9	mA
	RE =5 V,No Load,DE =0 V,No Load				300	μA
Input current	Other input =0 V	VI=12 V			250	A
		VI=12V Vcc=0			250	
		VI=-7V	-200			
		VI=-7V Vcc=0	-200			
Ioz High-impedance-state output current	Vo=0.4V to 2.4 V				±100	μA
Vhys Input hysteresis voltage				70		mV
VT+Positive-going input threshold voltage					200	mV
VIT-Negative-going input threshold voltage			-200			mV
VOH High-level output voltage	IoH=-8mA Figure 7		2.8			V
VoLLow-level output voltage	IoL=4 mA Figure 7				0.4	V

All typical values are at VCC =5V,TA=25℃.

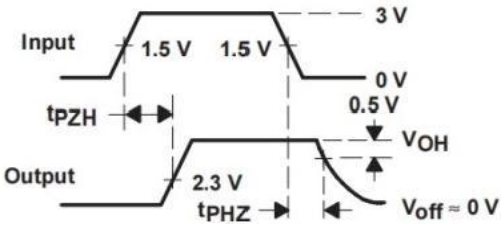
switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH Propagation delay time,low-to-high-level output	CL=50 pF,See Figure 7			150	ns
tPHL Propagation delay time,high-to-low-level output				150	ns
tsk(p)Pulse skew (ItpHL-tpLHI)				50	ns
tr Rise time,single ended	See Figure 7		20		ns
tf Fall time,single ended			20		ns
tPZH Output enable time to high level	See Figure 8			100	ns
tPZL Output enable time to low level				100	ns
tPHZ Output disable time from high level				100	ns
tPLZ Output disable time from low level				100	ns

PARAMETER MEASUREMENT INFORMATION



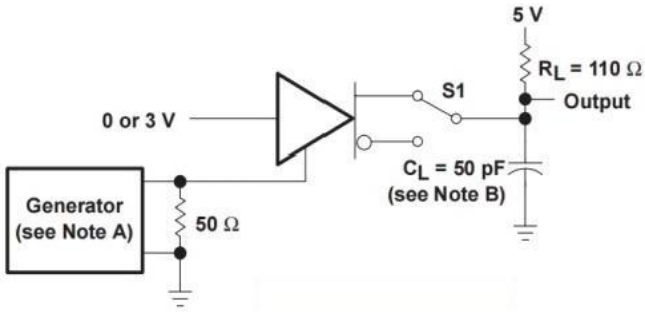
TEST CIRCUIT



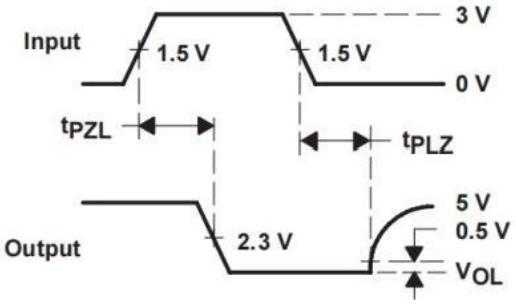
VOLTAGE WAVEFORMS

NOTES:
A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, tr ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
B. CL includes probe and jig capacitance.

Figure 2. Driver t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



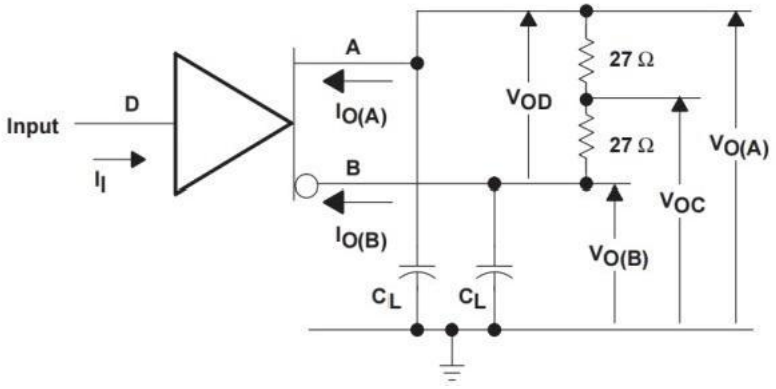
TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns, ZO = 50 Ω.
B. CL includes probe and jig capacitance.

Figure 3. Driver t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms



NOTES:
A. Resistance values are in ohms and are 1% tolerance.
B. CL includes probe and jig capacitance.

Figure 4. Driver Test Circuit, Voltage, and Current Definitions

PARAMETER MEASUREMENT INFORMATION

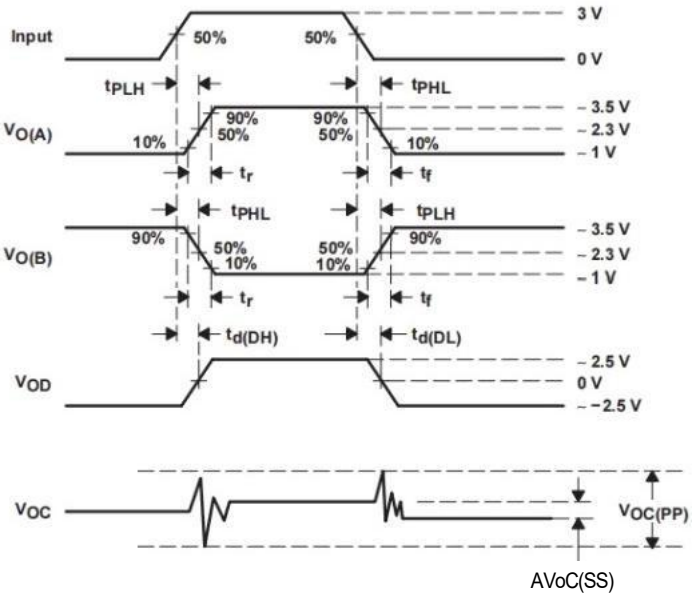
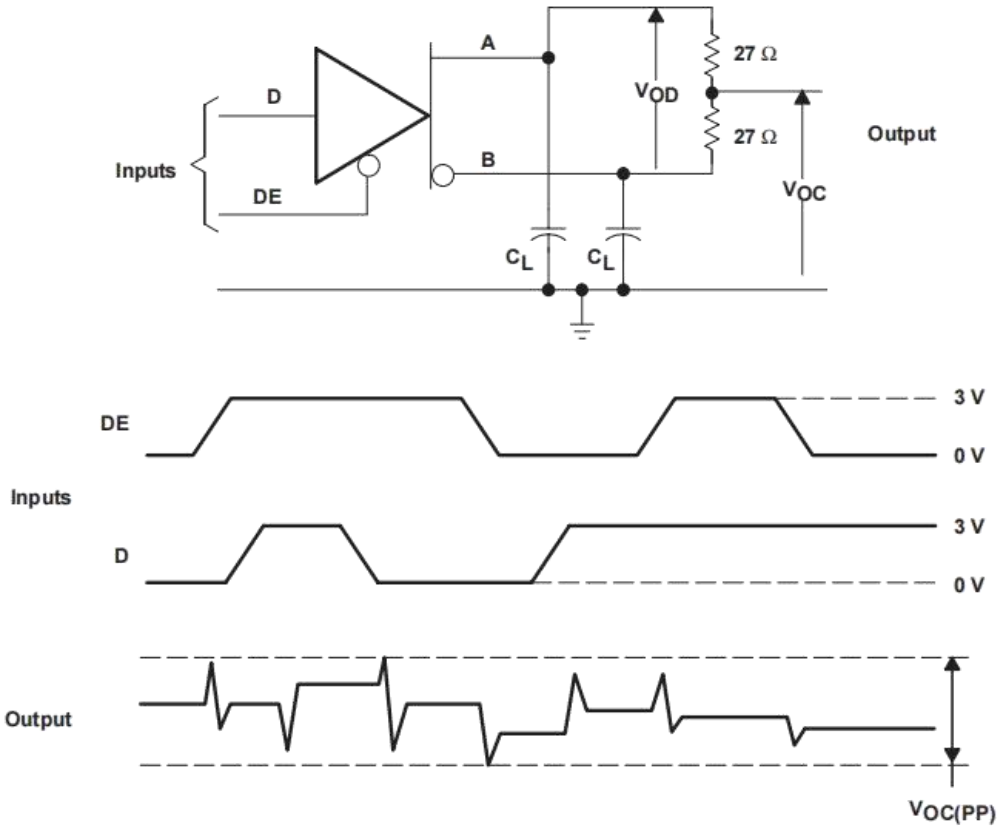


Figure 5.Driver Timing,Voltage and Current Waveforms

PARAMETER MEASUREMENT INFORMATION

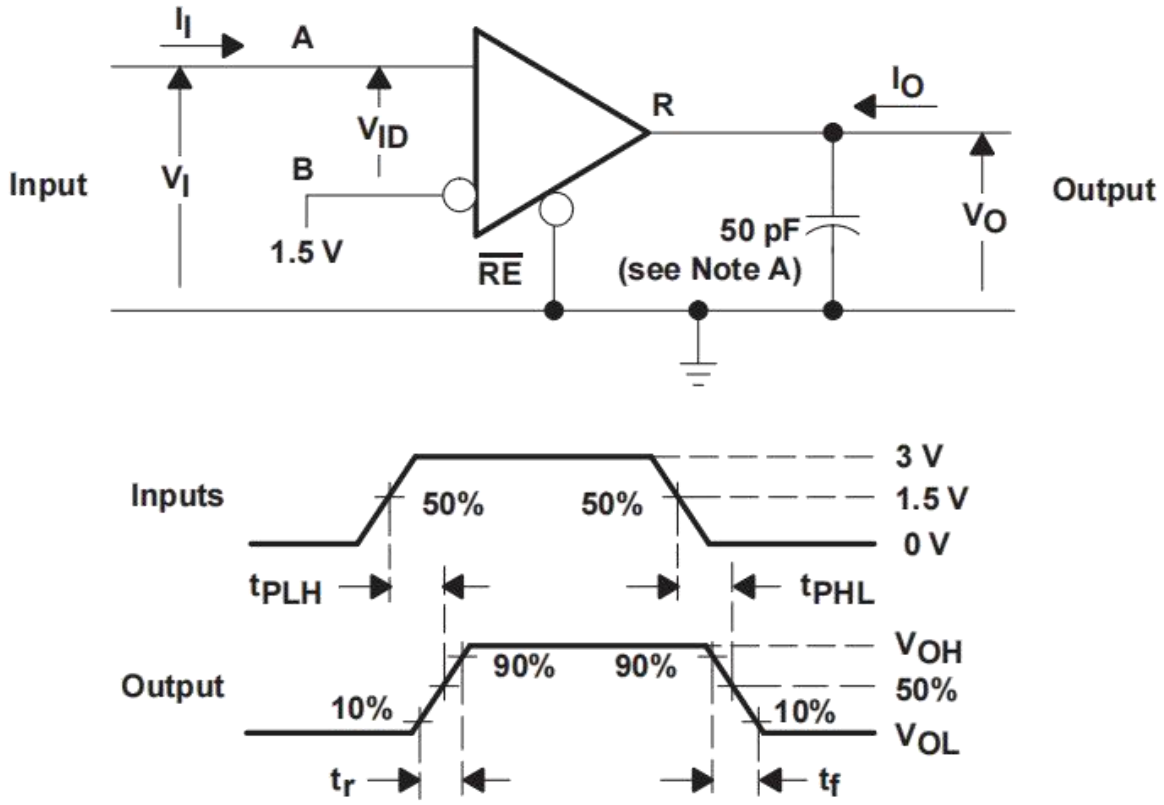


NOTES:

A. Resistance values are in ohms and are 1%tolerance.

B. CL indudes probe and jig capacitance (±10%).

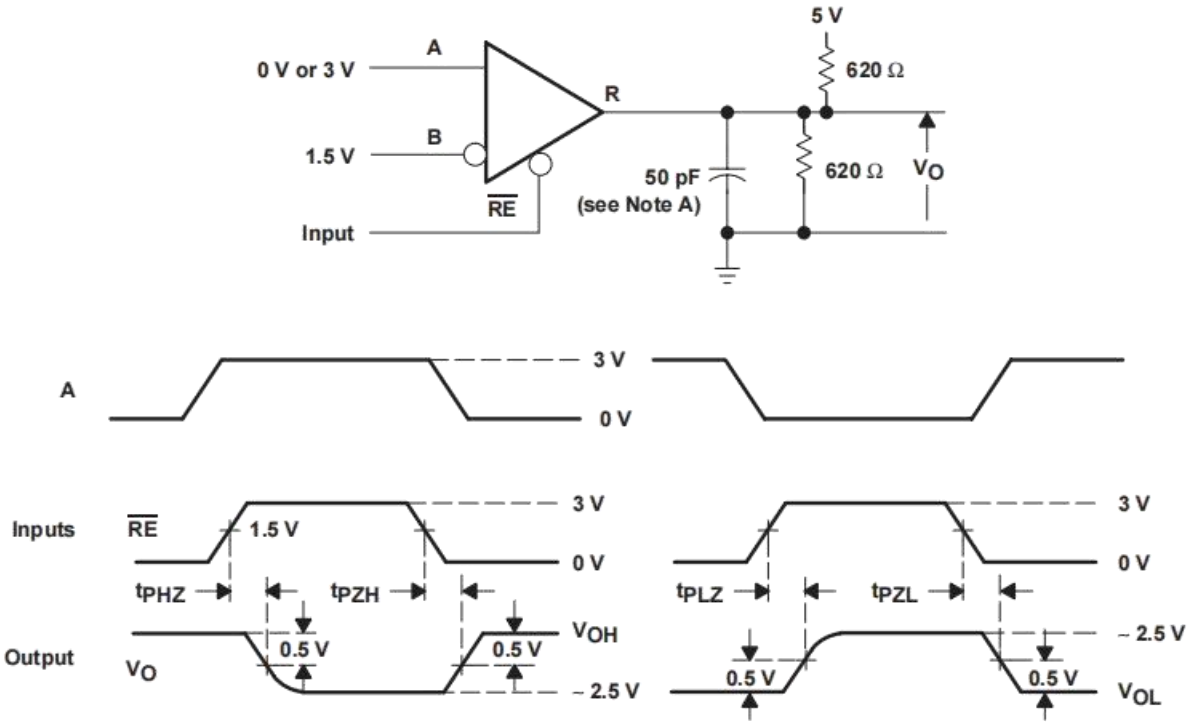
Figure 6. Driver $V_{OC(PP)}$ Test Circuit and Waveforms



NOTEA: This value includes probe and jig capacitance (± 10%).

Figure 7. Receiver t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTEA: This value includes probe and jig capacitance (± 10%).

Figure 8. Receiver t_{PZL}, t_{PLZ}, t_{PZH}, and t_{PHZ} Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

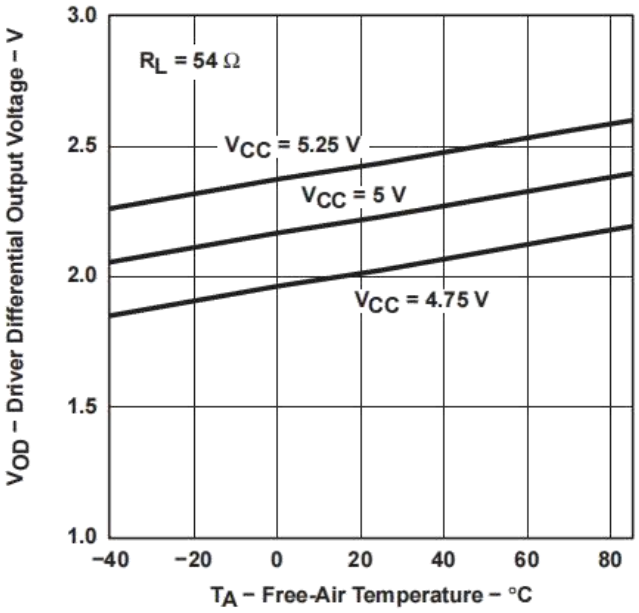


Figure 9

DRIVER PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

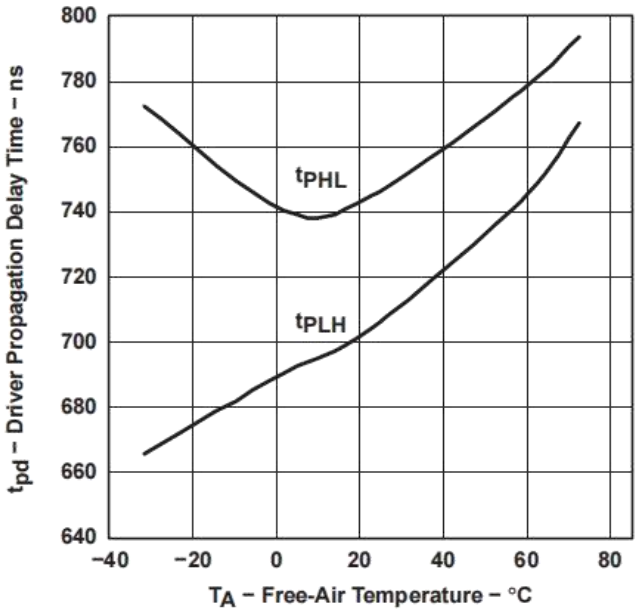


Figure 10

DRIVER TRANSITION TIME
vs
FREE-AIR TEMPERATURE

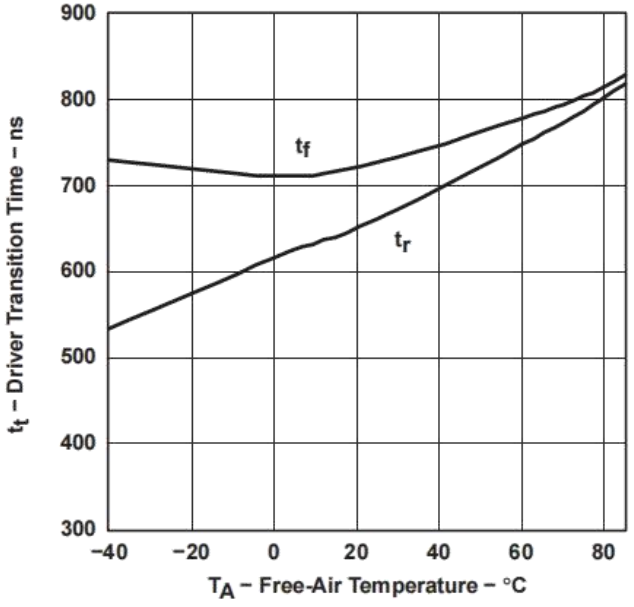


Figure 11

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

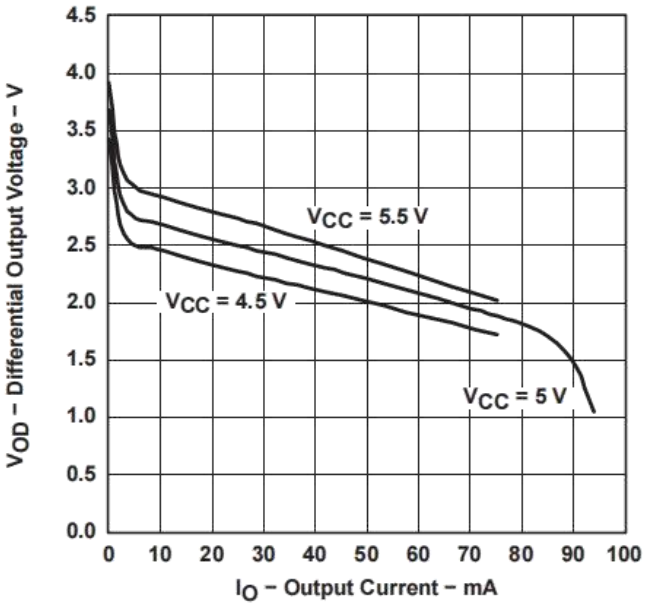


Figure 12

TYPICAL CHARACTERISTICS

RECEIVER INPUT CURRENT
VS
INPUT VOLTAGE

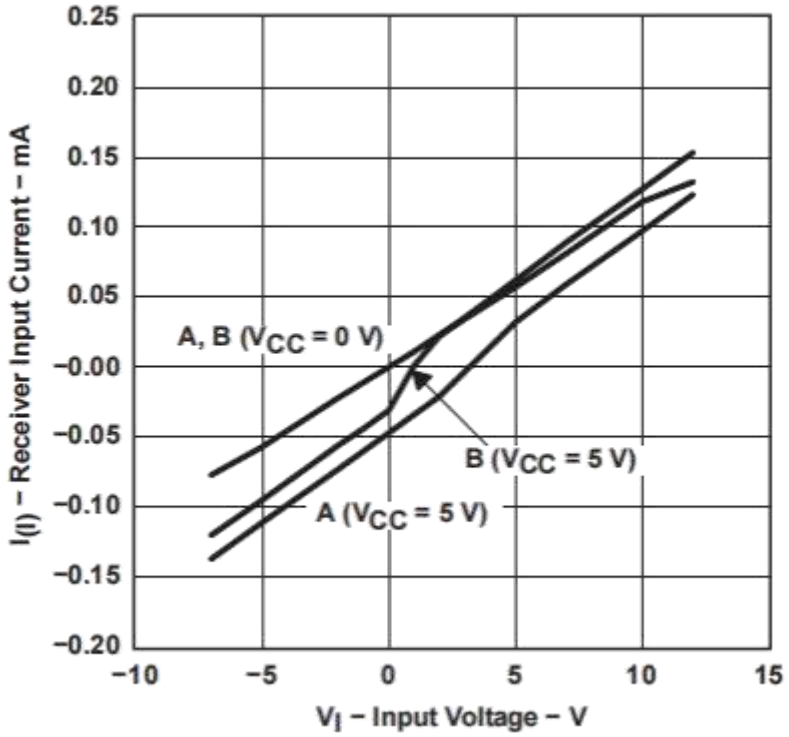
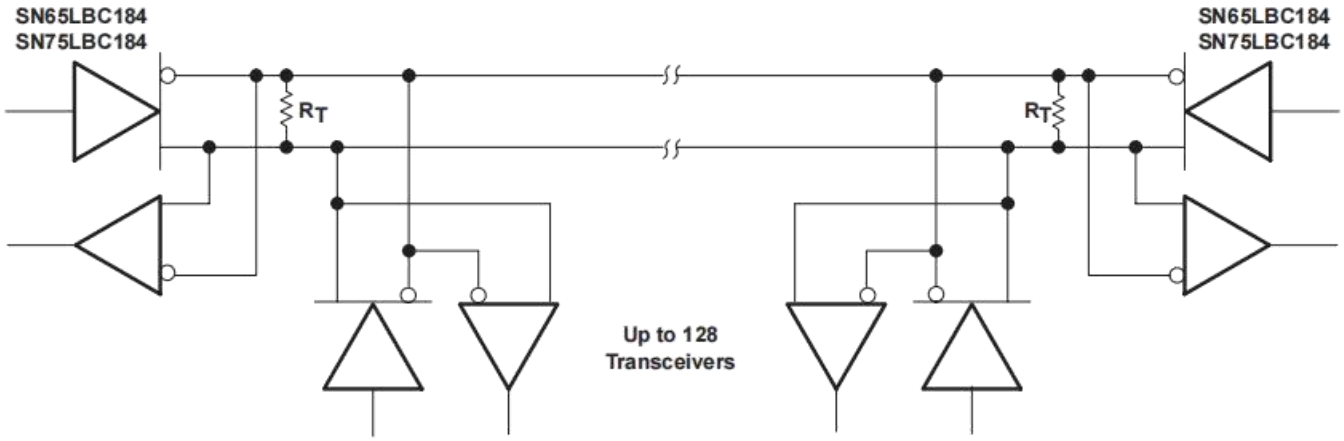


Figure 13

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance (RT = ZO). Stub lengths off the main line should be kept as short as possible.

Figure 14. Typical Application Circuit

APPLICATION INFORMATION

'LBC184 test description

The 'LBC184 is tested against the IEC 61000−4−5 recommended transient identified as the combination wave. The combination wave provides a 1.2-/50-μs open-circuit voltage waveform and a 8-/20-μs short-circuit current waveform shown in Figure 15. The testing is performed with a combination/hybrid pulse generator with an effective output impedance of 2 Ω. The setup for the overvoltage stress is shown in Figure 16 with all testing performed with power applied to the 'LBC184 circuit.

NOTE

High voltage transient testing is done on a sampling basis.

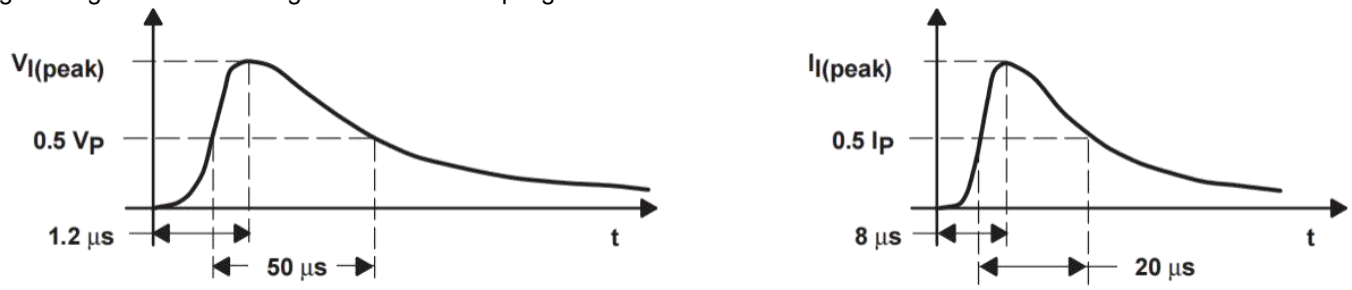


Figure 15. Short-Circuit Current Waveforms

The 'LBC184 is tested and evaluated for both maximum (single pulse) as well as life test (multiple pulse) capabilities. The 'LBC184 is evaluated against transients of both positive and negative polarity and all testing is performed with the worst-case transient polarity. Transient pulses are applied to the bus pins (A & B) across ground as shown in Figure 16.

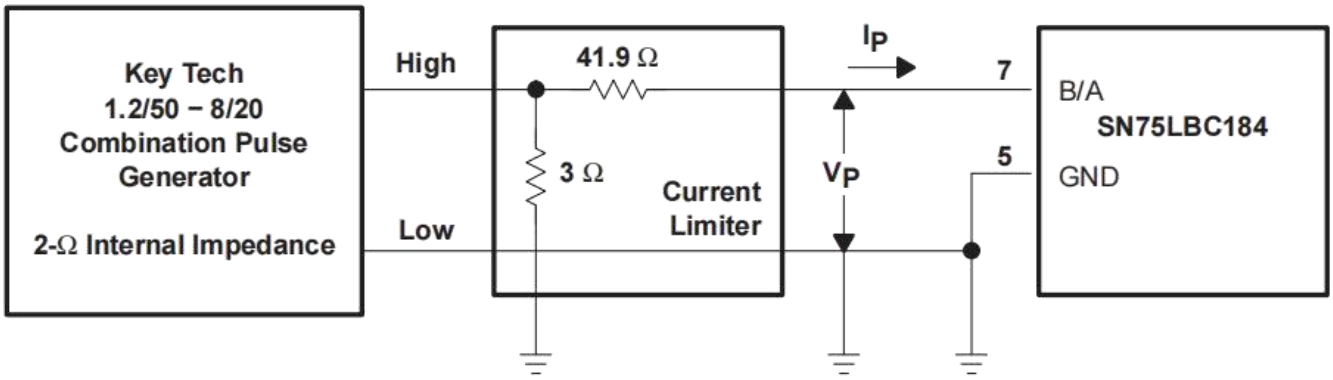


Figure 16. Overvoltage-Stress Test Circuit

An example waveform as seen by the 'LBC184 is shown in Figure 17. The bottom trace is current, the middle trace shows the clamping voltage of the device and the top trace is power as calculated from the voltage and current waveforms. This example shows a peak clamping voltage of 16 V, peak current of 33.6 A yielding an absorbed peak power of 538 W.

NOTE

A circuit reset may be required to ensure normal data communications following a transient noise pulse of greater than 250 W peak.

APPLICATION INFORMATION

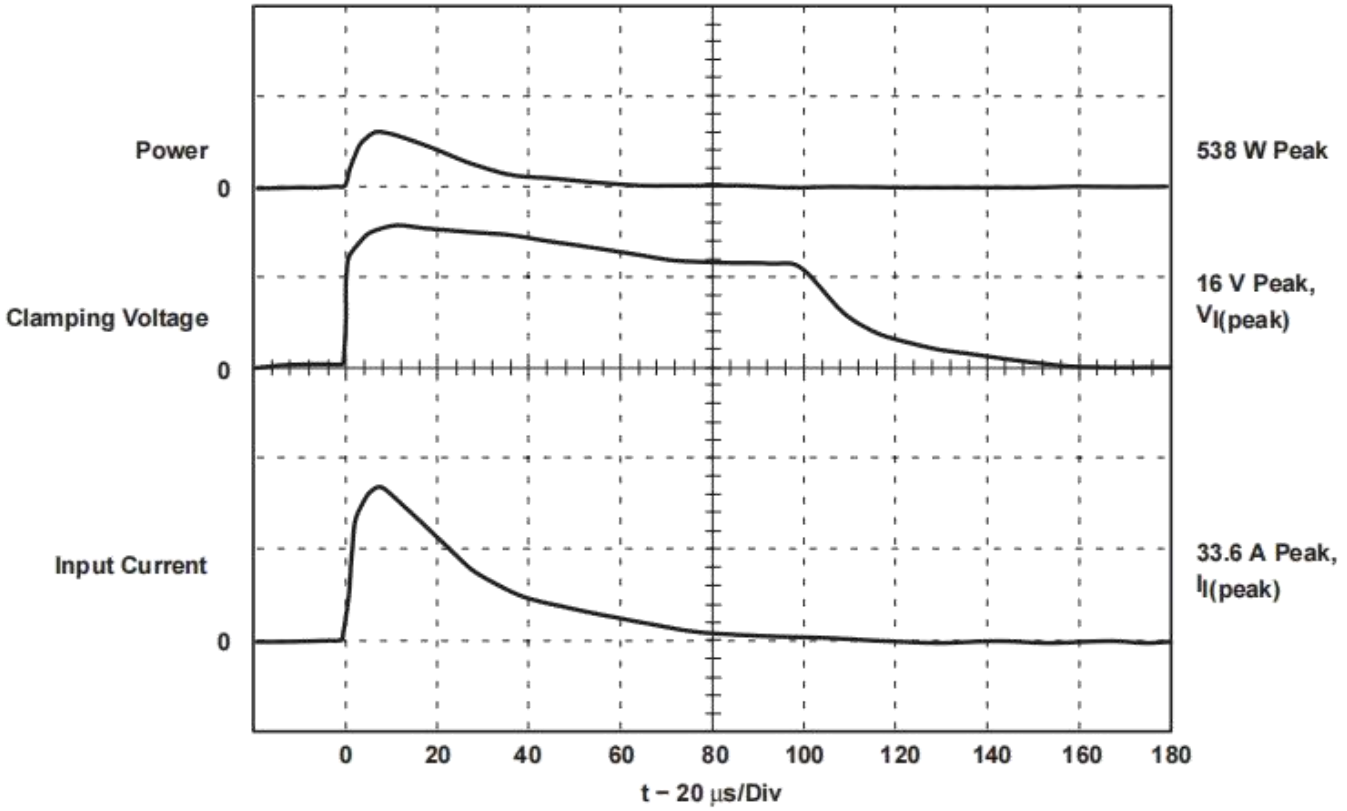
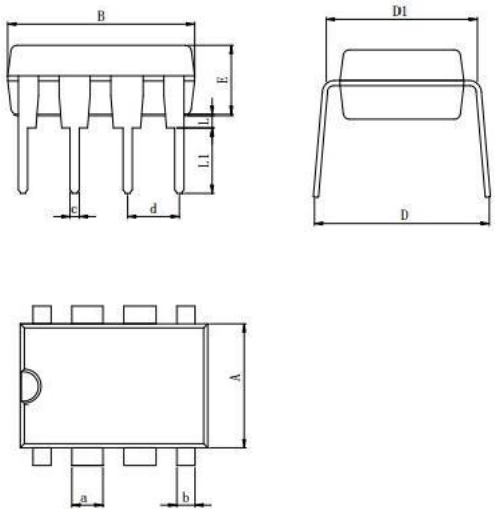


Figure 17. Typical Surge Waveform Measured At Terminals 5 and 7

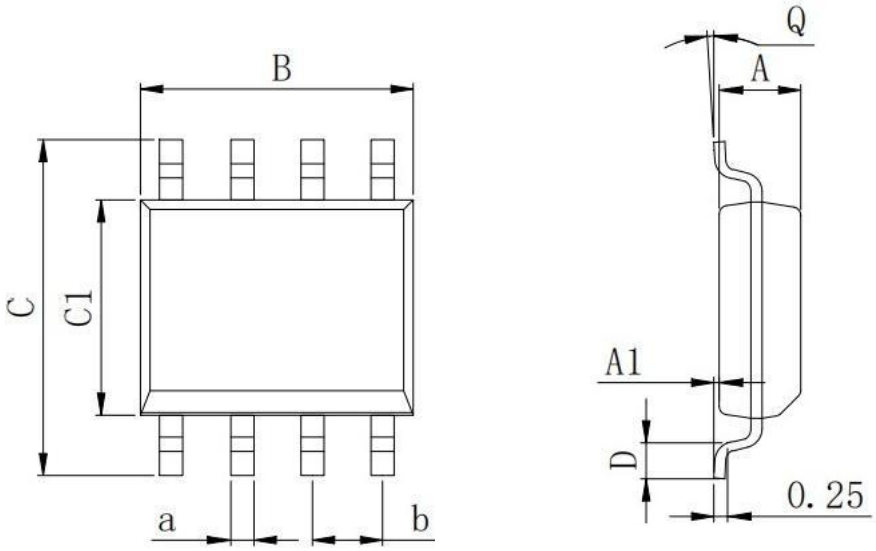
Physical Dimensions

DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	**A**	B	D	D1	E	L	**L1**	**a**	**b**	**C**	**d**
Min:	6.10	9.00	8.10	7.42	3.10	0.50	**3.00**	**1.50**	**0.85**	**0.40**	**2.54 BSC**
Max:	6.68	9.50	10.9	7.82	3.55	0.70	**3.60**	**1.55**	**0.90**	**0.50**	

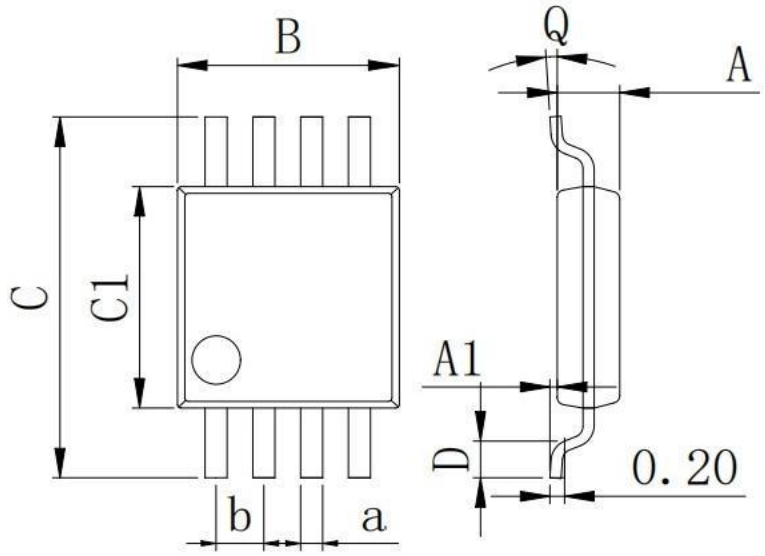
SOP-8 (150min)



Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	**B**	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	**0.40**	**0°**	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	**0.80**	8°	0.45	

Physical Dimensions

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	